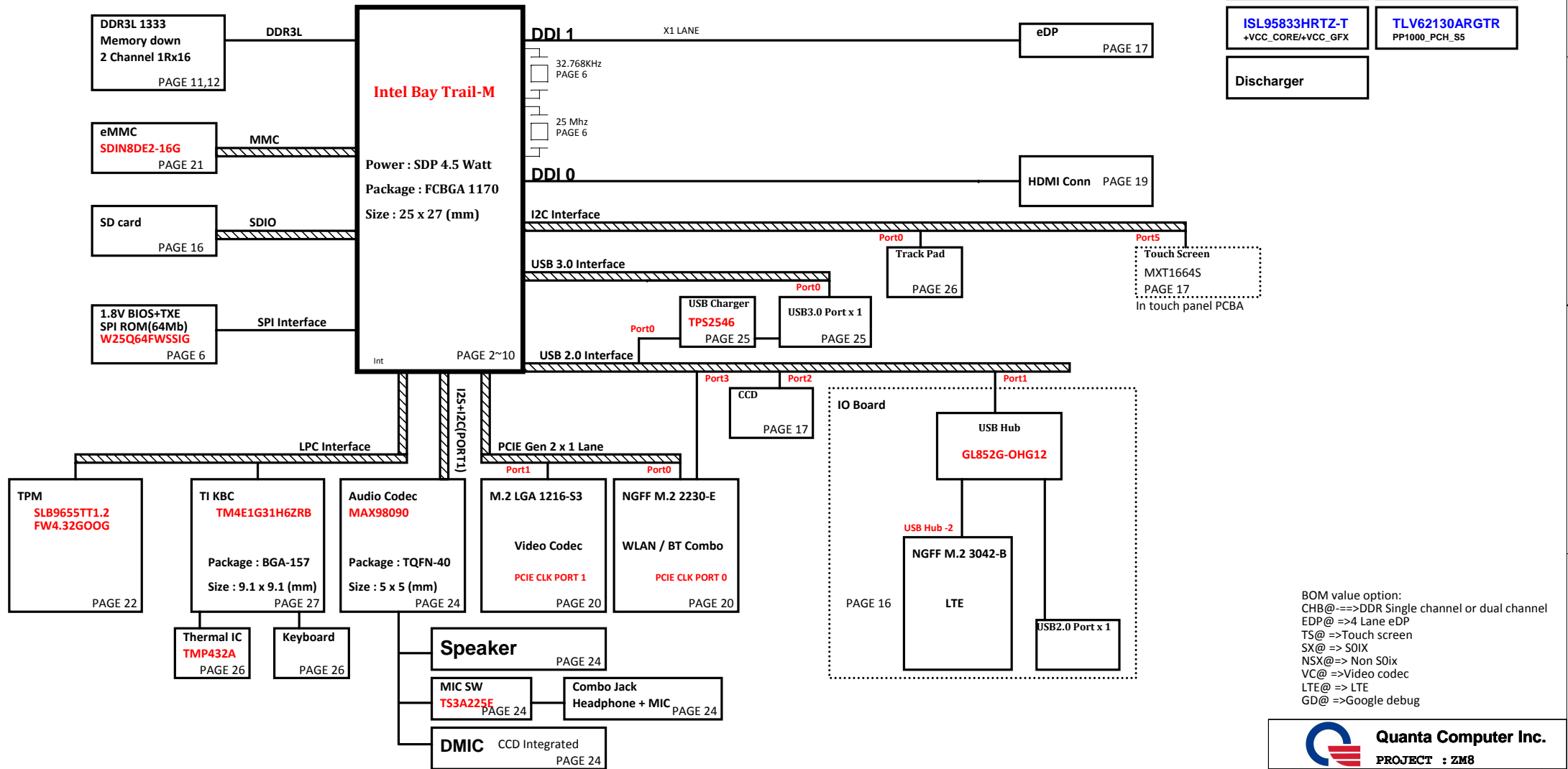
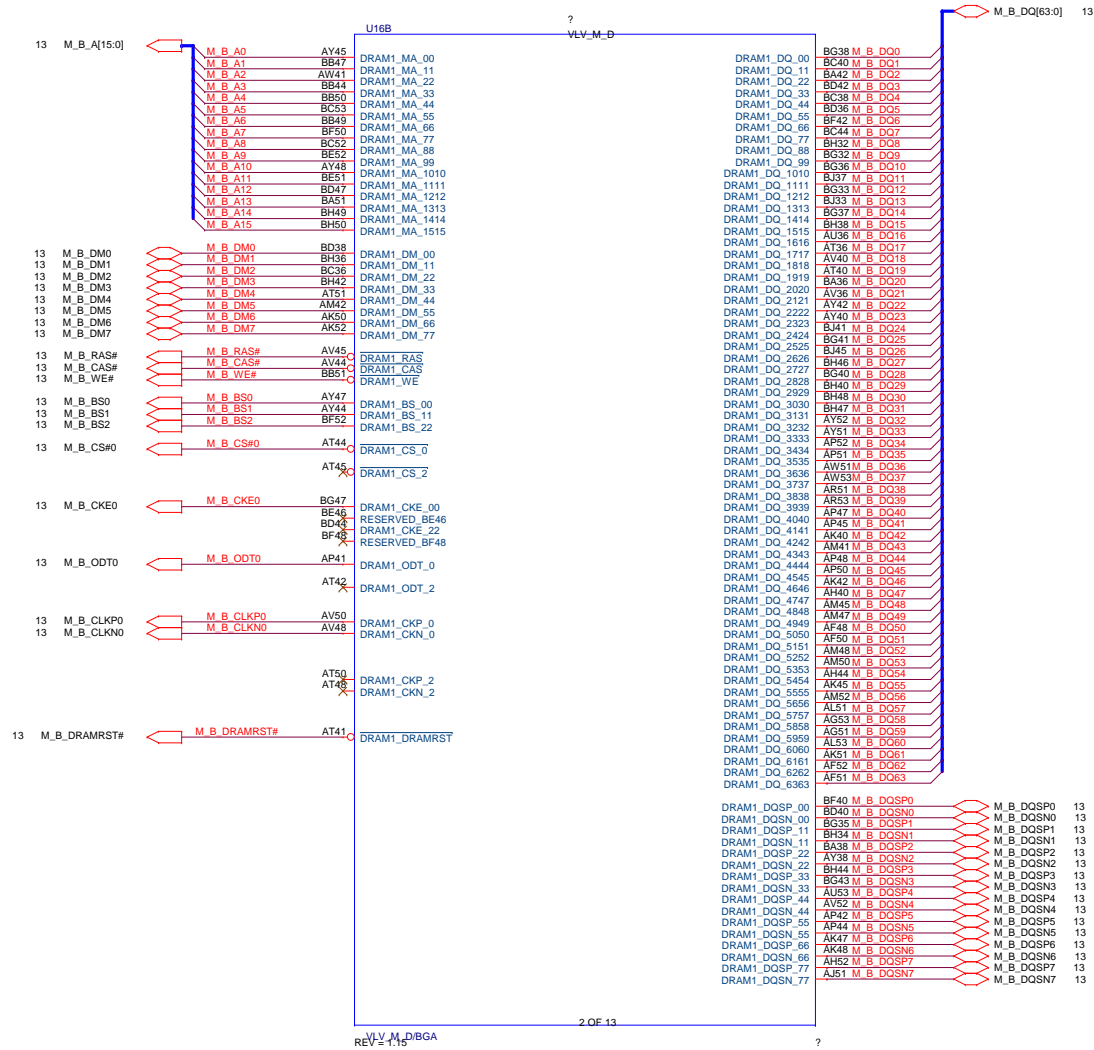


## Intel Bay Trail-M Platform Block Diagram

EVT  
AJSR1YJUT07--CPU(1170P)N2840 2.16G SR1YJ(FCBGA)WINBSQ

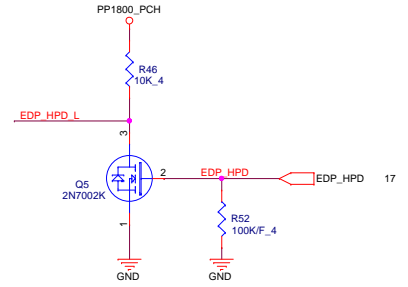
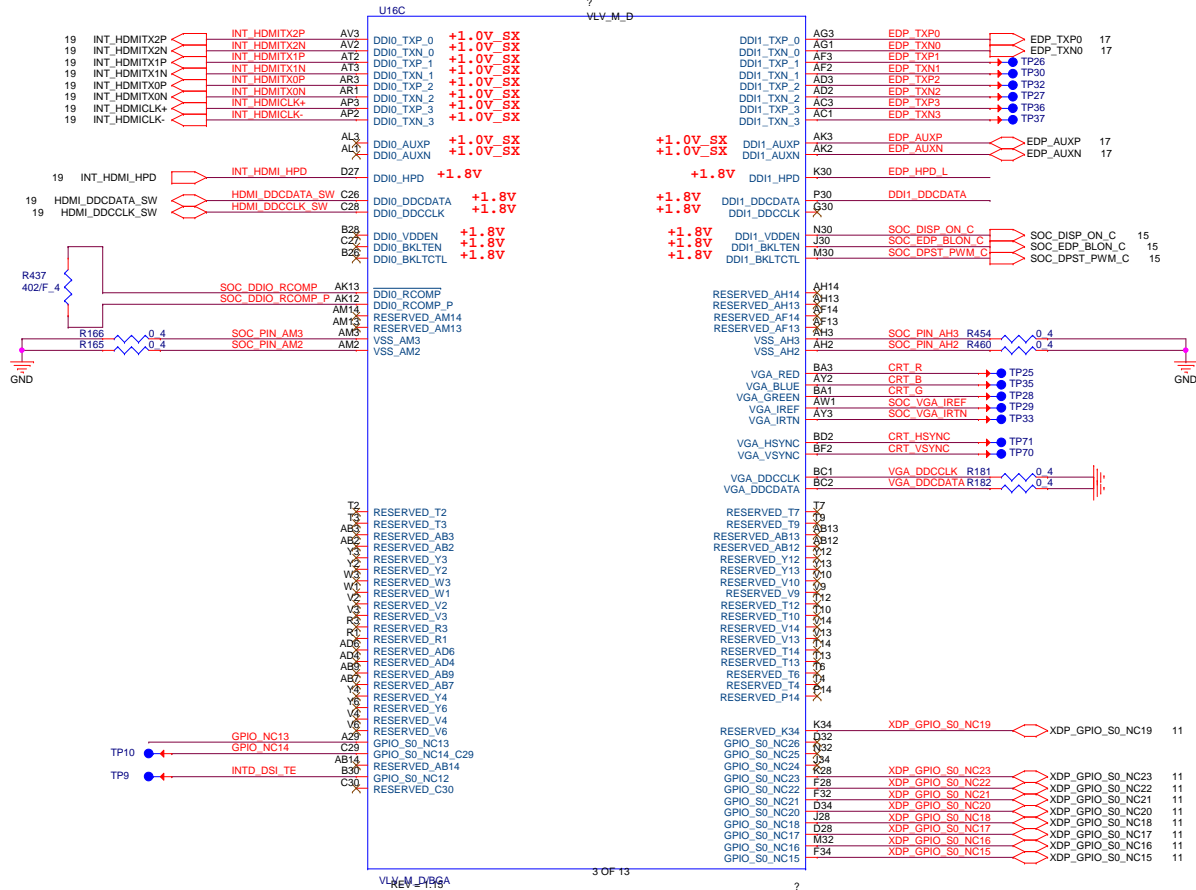






# SoC (CPU)

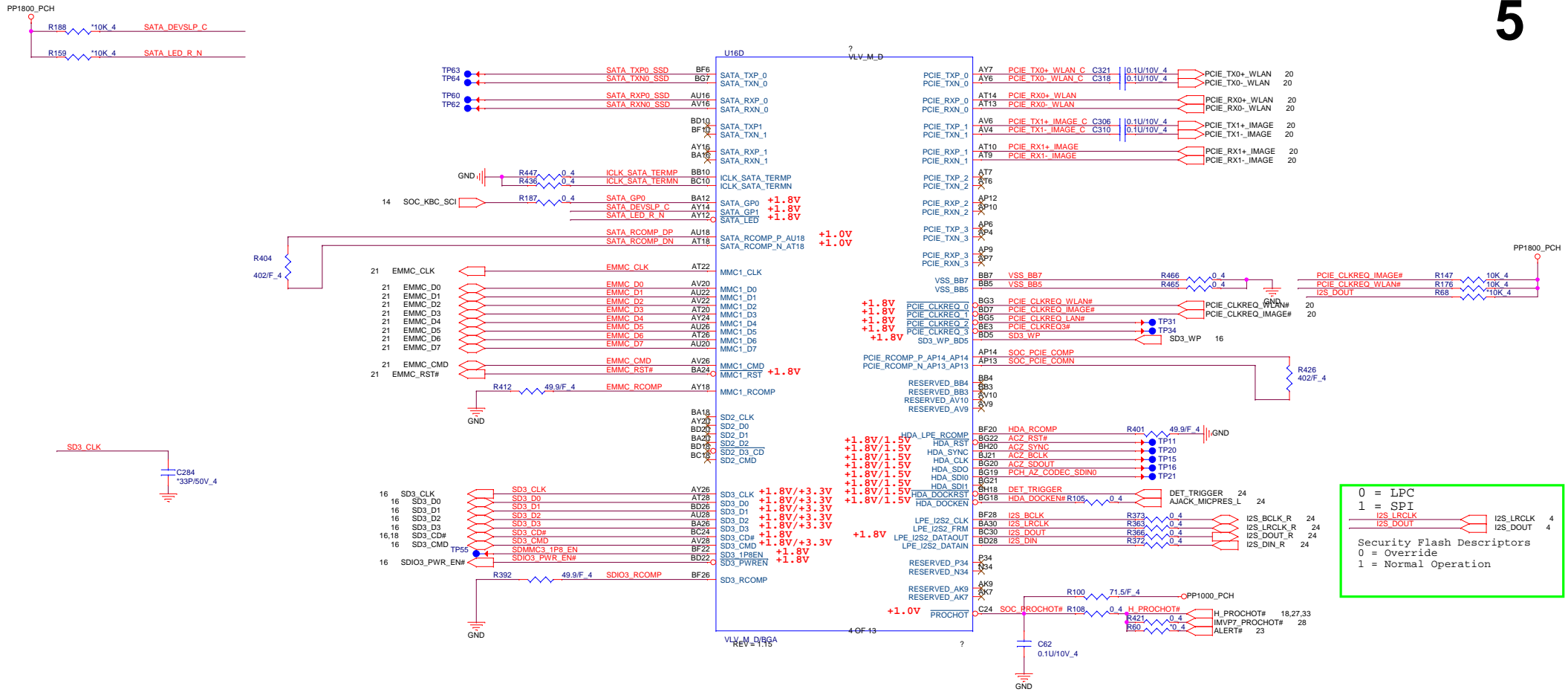
4



BTM Strapping Table

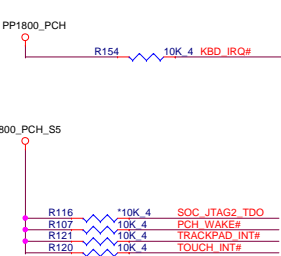
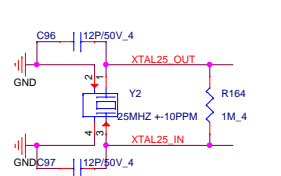
Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is inverted 1 = Top address bit is unchanged	7 GPIO_SO_SC_56 PP1800_PCH R438 10K_4 R429 10K_4 GND
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	5 I2S_LRCLK PP1800_PCH R364 10K_4 R361 10K_4 GND
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	5 I2S_DOUT 27 SOC_OVERRIDE# R58 0.4 SOC_OVERRIDE NM 2 GND
DDIO_DDCDATA	DDIO Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	Pull up +1.8V at HDMI side DDIO_DDCDATA SW R85 10K_4 GND
DDH1_DDCDATA	DDH1 Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	DDH1_DDCDATA PP1800_PCH R378 2.2K_4 R378 10K_4 GND
GPIO_SO_NC_13				GPIO_NC13 PP1800_PCH R75 10K_4 R80 10K_4 GND

# SoC (CPU)

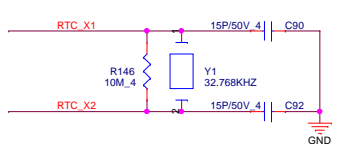


0 = LPC  
1 = SPI  
I2S\_LRCLK  
I2S\_DOUT  
Security Flash Descriptors  
0 = Override  
1 = Normal Operation

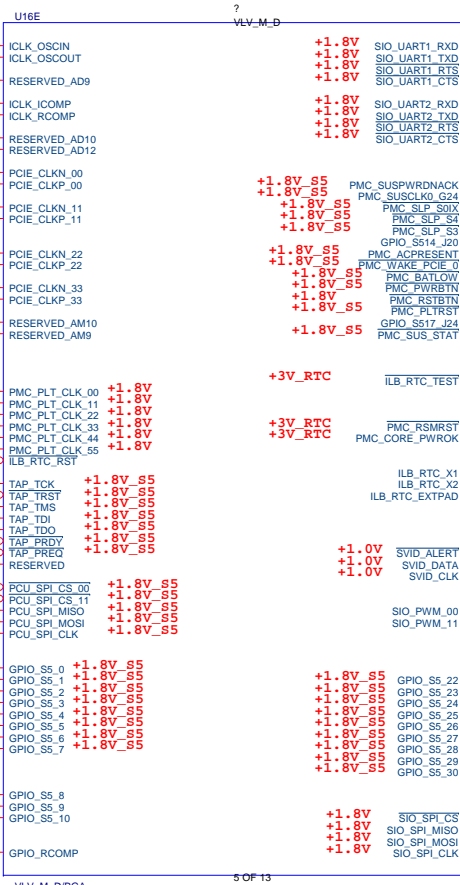
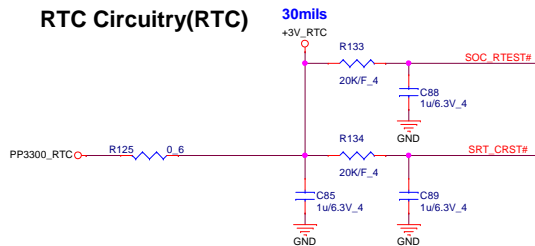
# SoC (CPU)



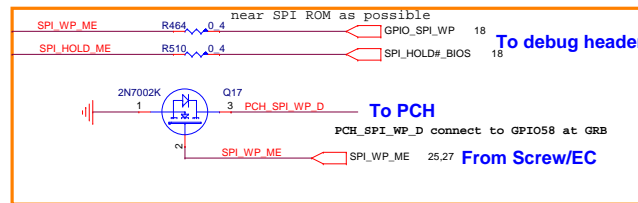
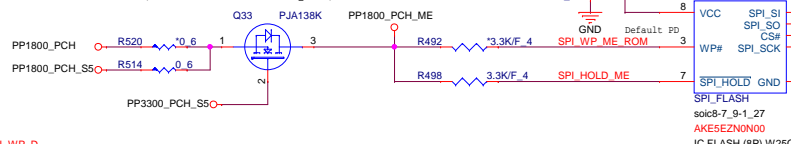
## RTC Clock 32.768KHz



## RTC Circuitry(RTC)

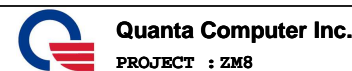


SPI ROM needs power in S3/S5 for the TXE (Trusted execution engine).



## SPI NOR FLASH

Need unstuff once SEL debug port is un-stuffed

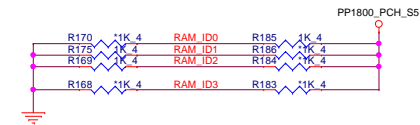


Size	Document Number	Rev
	Valley 5/9 (SPI/GPIO/CLK)	1A
Date:	Thursday, September 25, 2014	Sheet 6 of 39

## SoC (CPU)

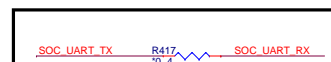
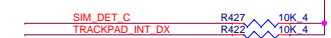
## RAM ID

7



Vender	RAM_ID	Q PN	Mfr. PN	Freq.	Size	Total Size
Micron	000	AKD5JGSLT02	MT41K256M16HA-125:E	1600MHz	4Gb	4GB
Hynix	001	AKD5JGETW00	H5TC4G63APR-PBA	1600MHz	4Gb	4GB
Samsung	010	AKD5PGST500	K4B4G1646Q-HYK0	1600MHz	4Gb	4GB
Samsung	011	AKD5PGST500	K4B4G1646Q-HYK0	1600MHz	4Gb	2GB
Micron	100	AKD5JGSLT02	MT41K256M16HA-125:E	1600MHz	4Gb	2GB
Hynix	101	AKD5JGETW00	H5TC4G63APR-PBA	1600MHz	4Gb	2GB

PP1800\_PCH



Un-Stuff for Test Only

PP1800\_PCH

Touch pad

Audio Codec

9/9 unstuff pull high resistor(R382, R380) of TP I2C signal

Light sensor

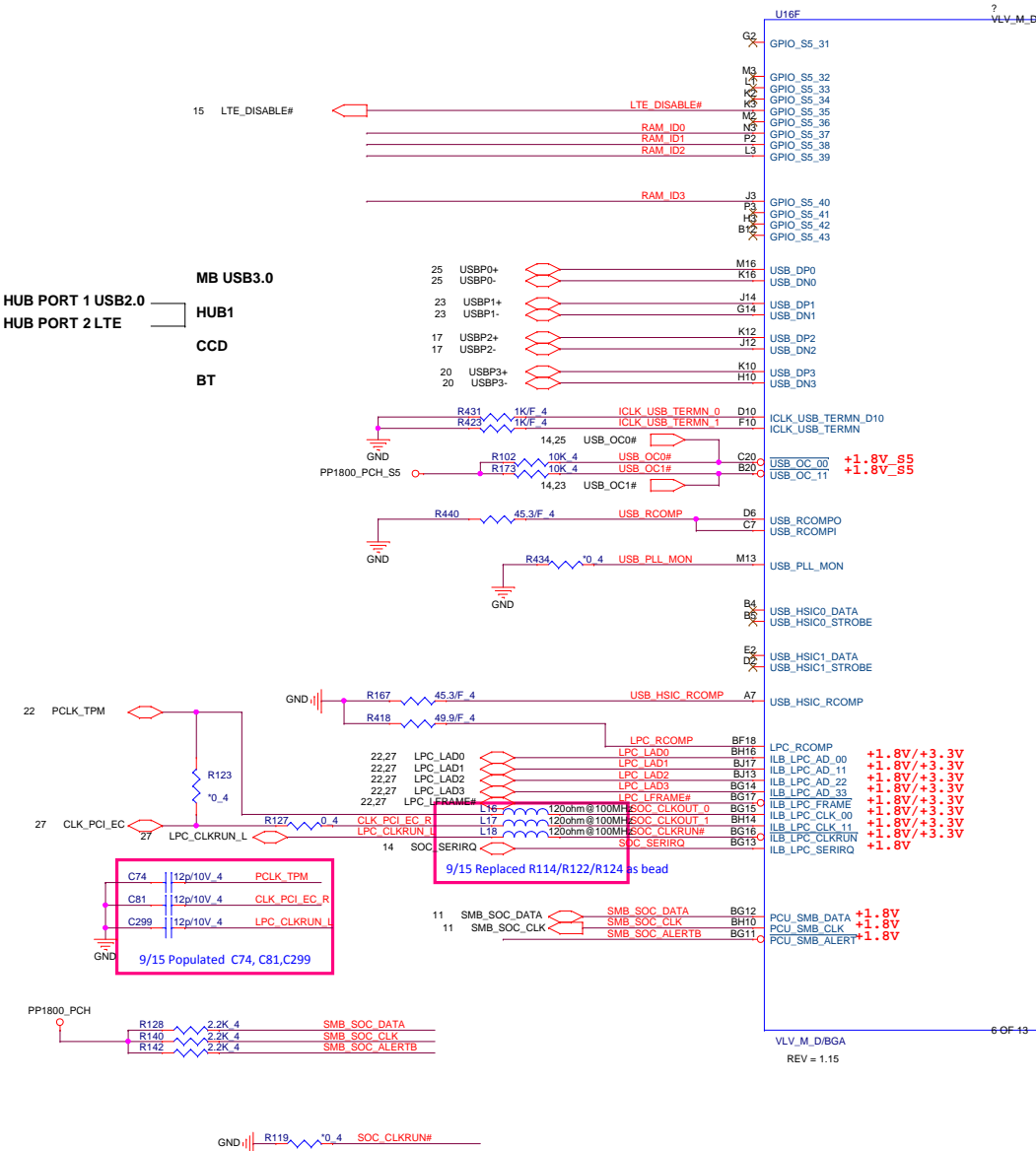
Touch panel



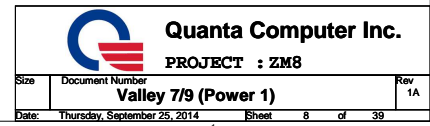
Quanta Computer Inc.

PROJECT : ZM8

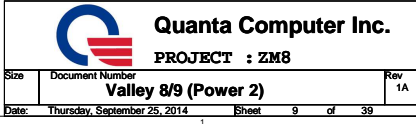
Size	Document Number	Rev
	Valley 6/9 (USB/LPC/I2C)	1A
Date:	Thursday, September 25, 2014	Sheet 7 of 39

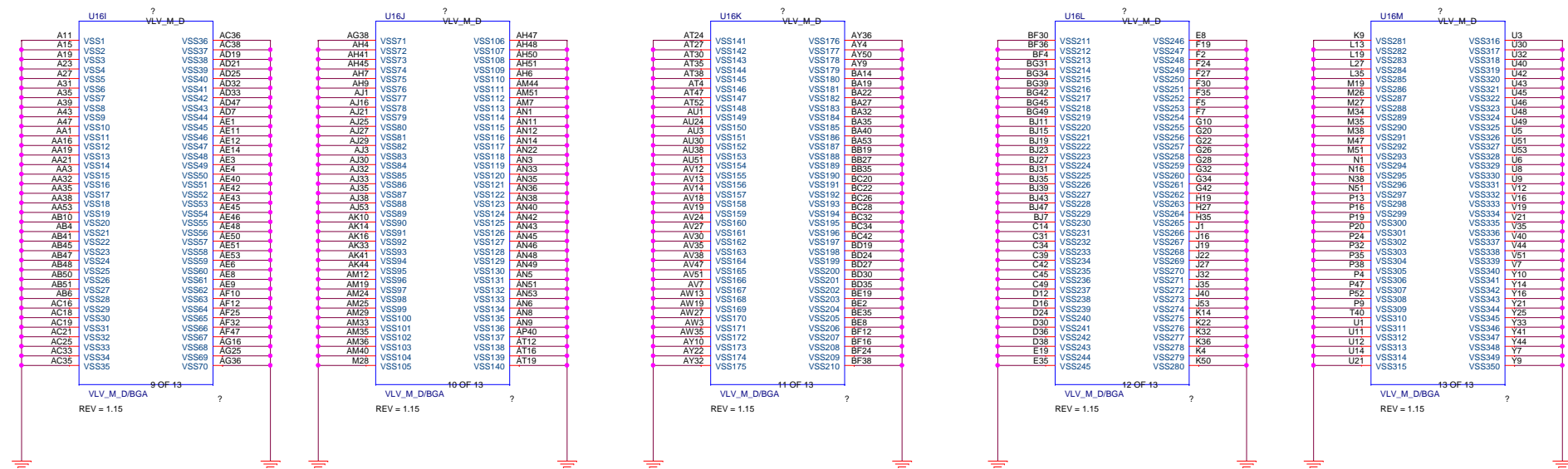


REV = 1.15

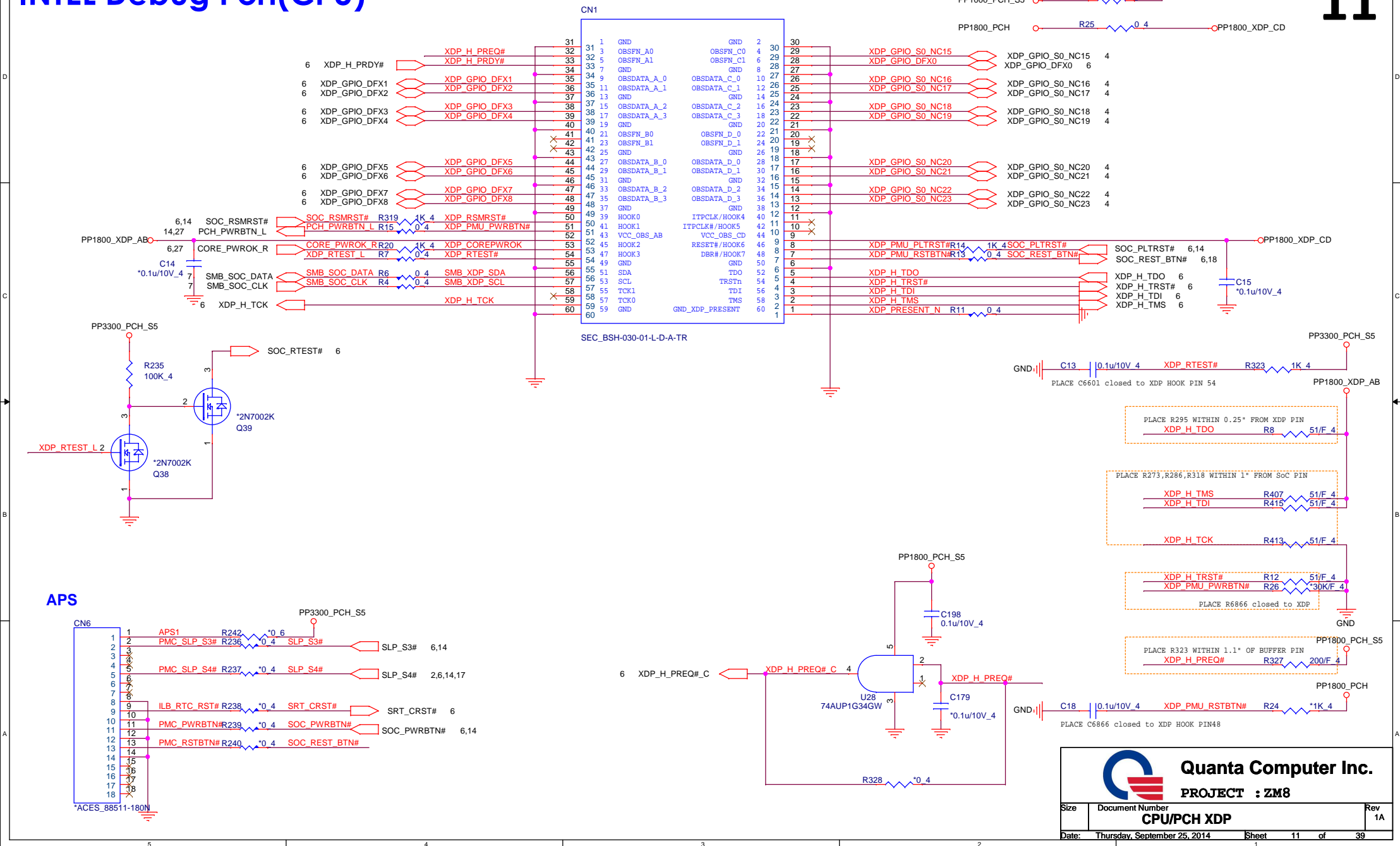


## 9

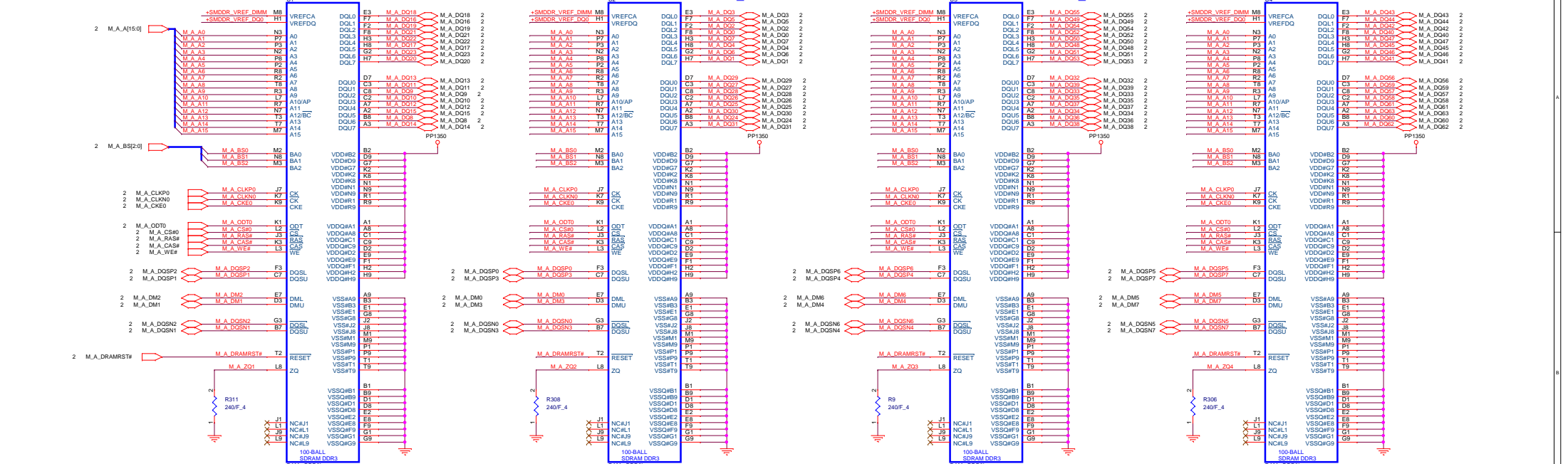




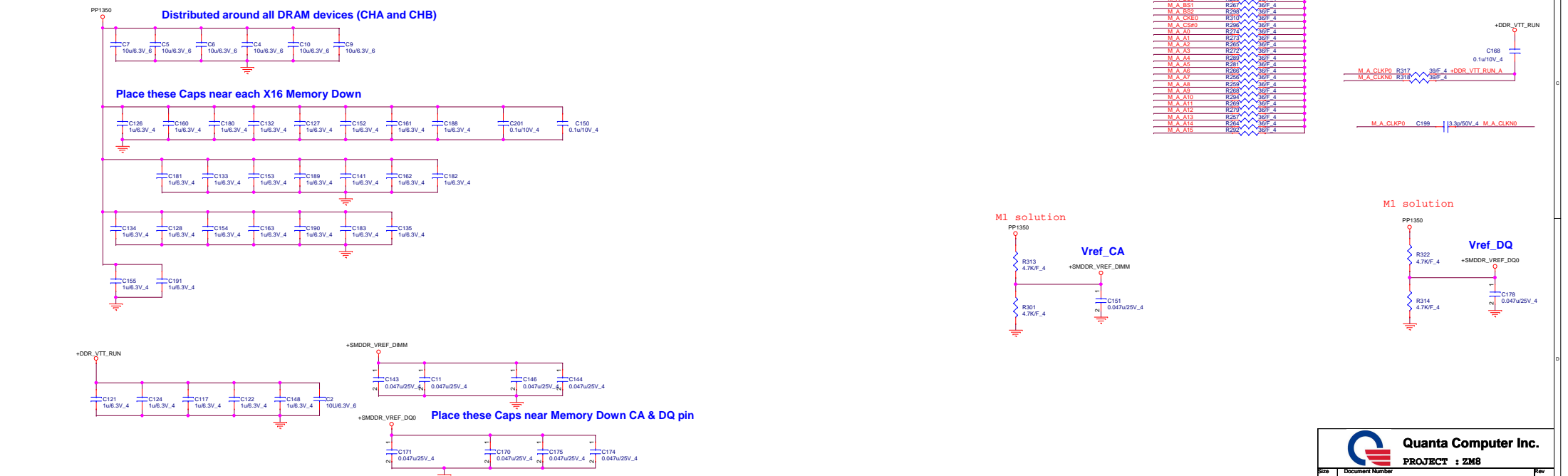
## 11



## On board memory (OBM)



Vendor	P/N	Mfr. P/N
Hynix	AKD5JGETW15 (WIN BSQ)	H5TC4G63AFR-PBA
Micron	AKD5JGSTL15 (WIN BSQ)	MT41K256M16HA-125:E
Samsung	AKD5PGST516 (WIN BSQ)	K4B4G1646Q-HYK0



# On board memory (OBM)

13

BYTE2\_16-23

BYTE3\_24-31

BYTE0\_0-7

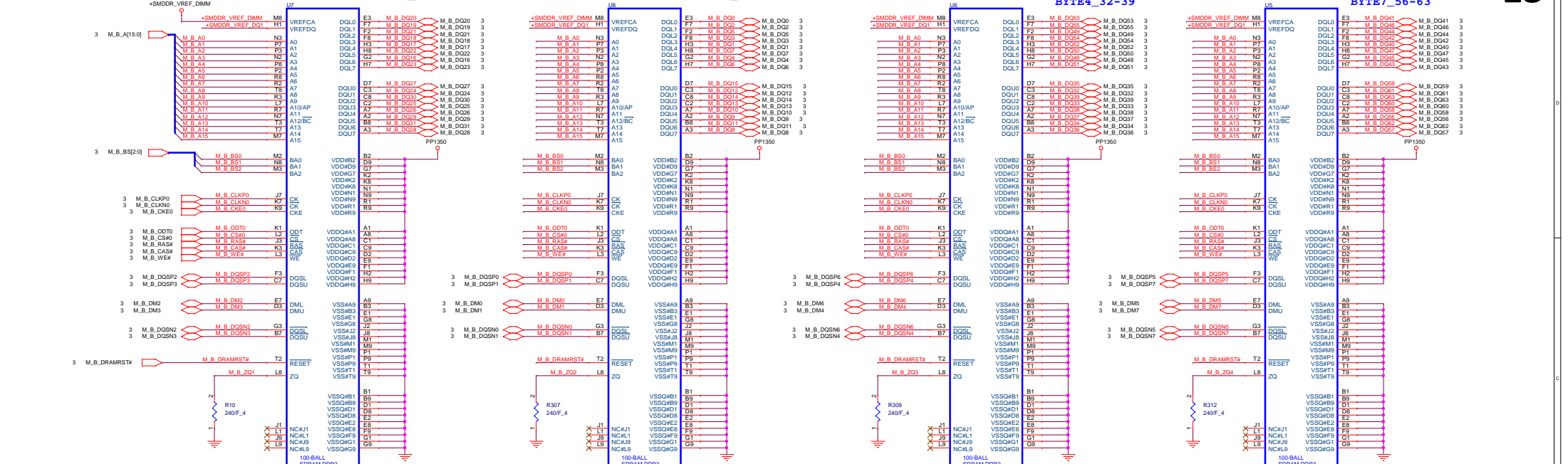
BYTE1\_8-15

BYTE6\_48-55

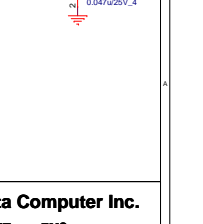
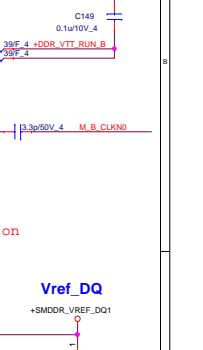
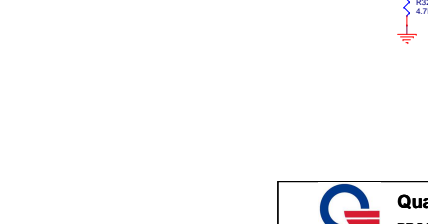
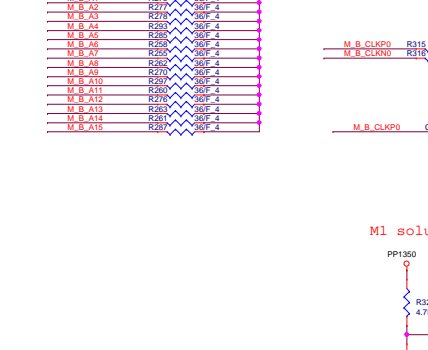
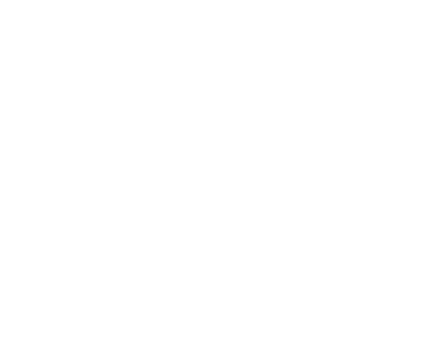
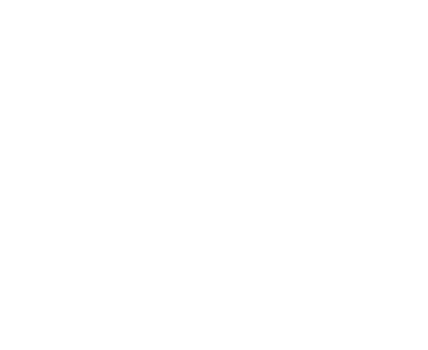
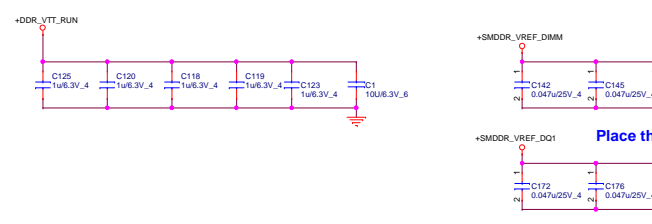
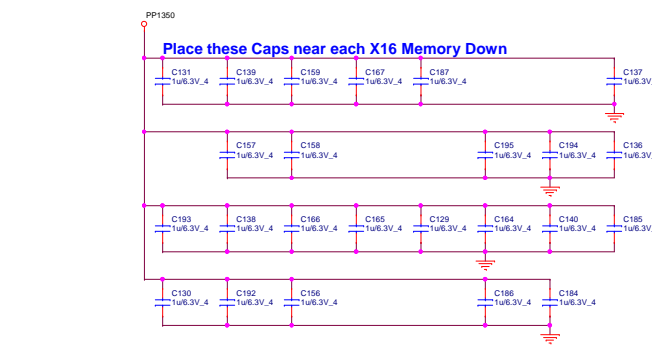
BYTE4\_32-39

BYTE5\_40-47

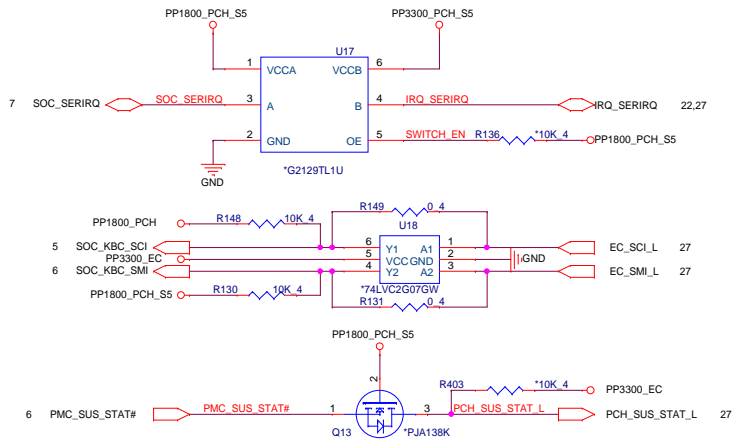
BYTE7\_56-63



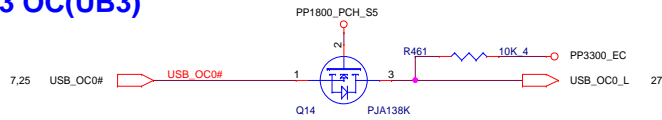
Vendor	P/N	Ref. P/N
Hynix	AKD5JGETW15 (WIN B5Q)	H5TC4G63AFR-PBA
Micron	AKD5JG5TL15 (WIN B5Q)	MT41K256M16HA-125:E
Samsung	AKD5PG5T516 (WIN B5Q)	K4B4G1646Q-HYK0



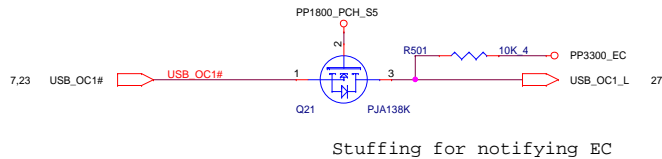
# PWRON SEQUENCE(CPU)



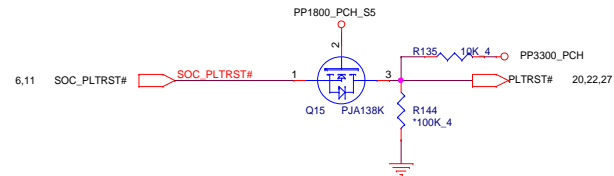
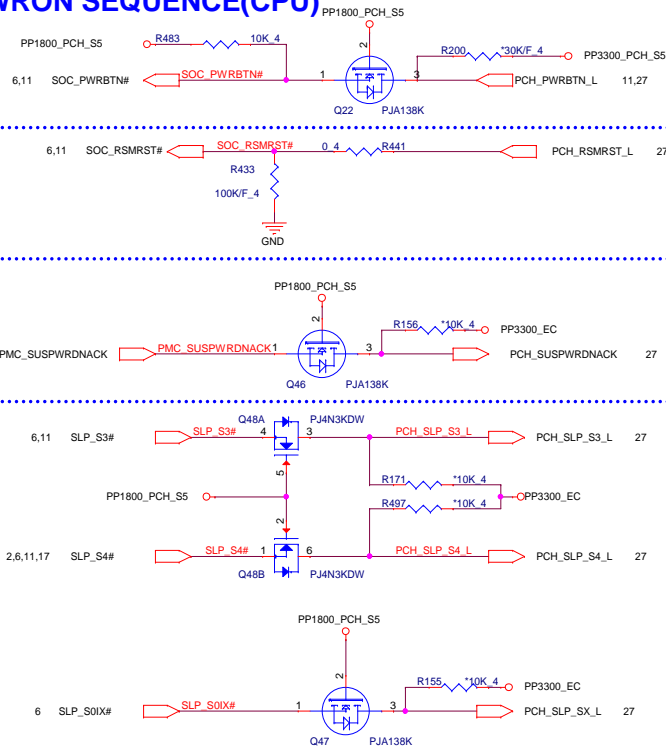
## USB3 OC(UB3)



## USB2 OC(UB2)

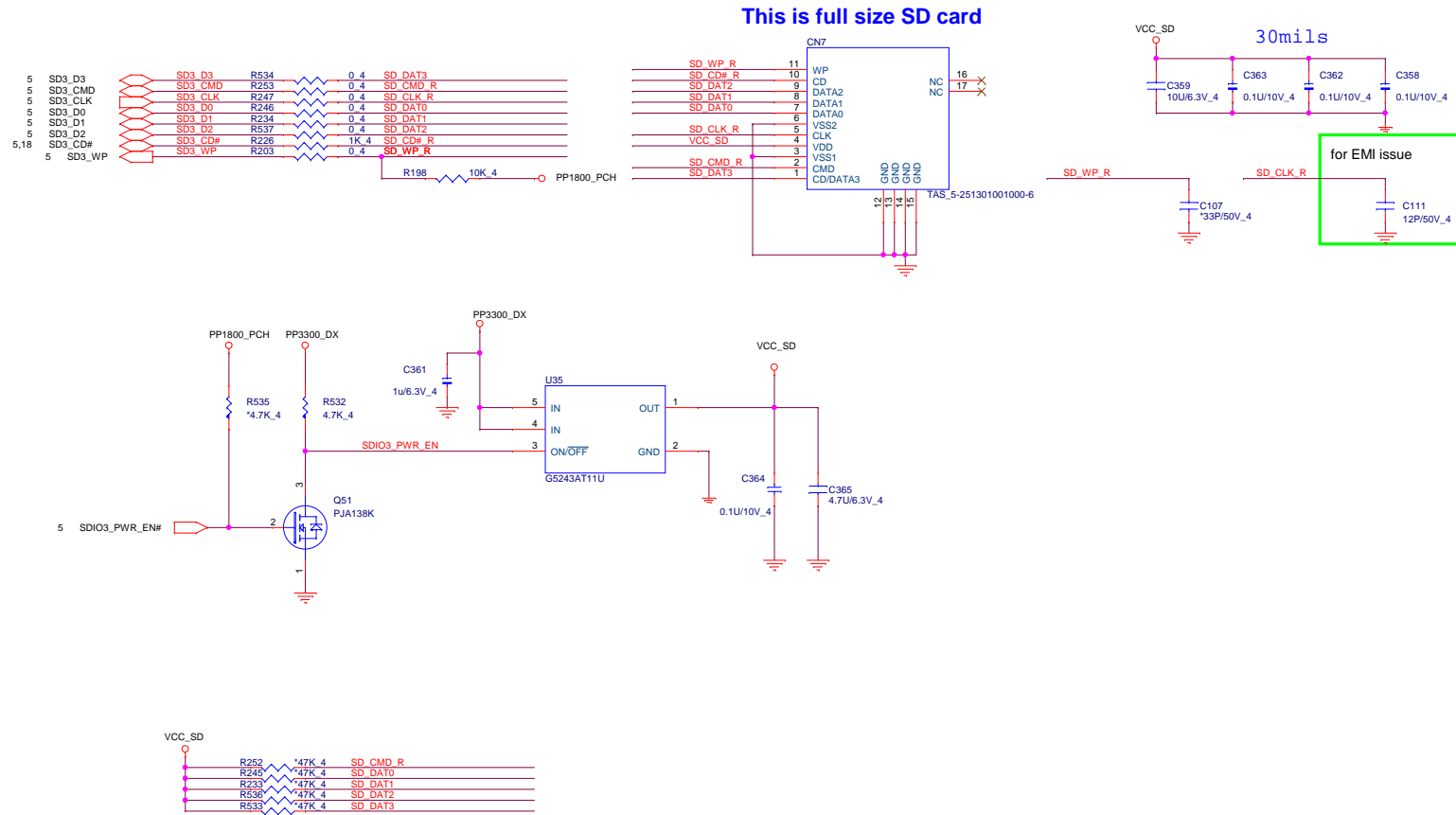


# PWRON SEQUENCE(CPU)

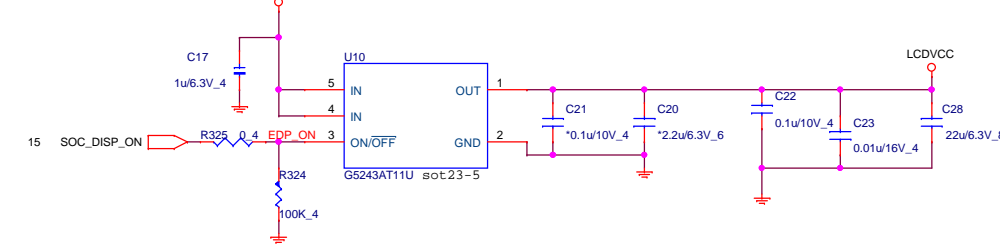




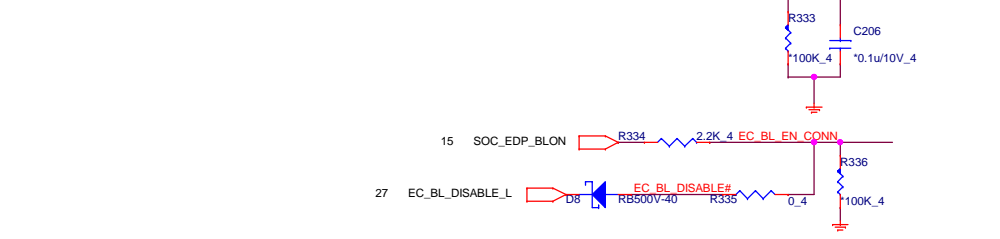
## SD/MMC CARD READER CONNECTOR (CRD)



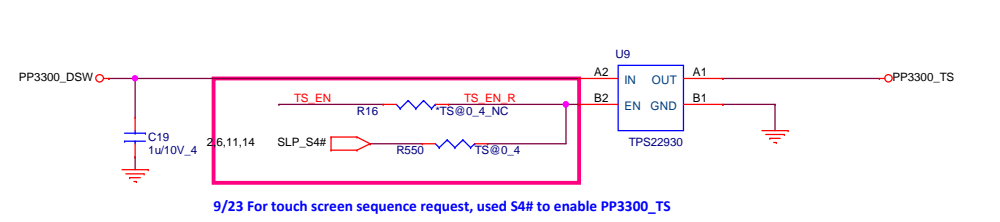
eDP Power(LDS)



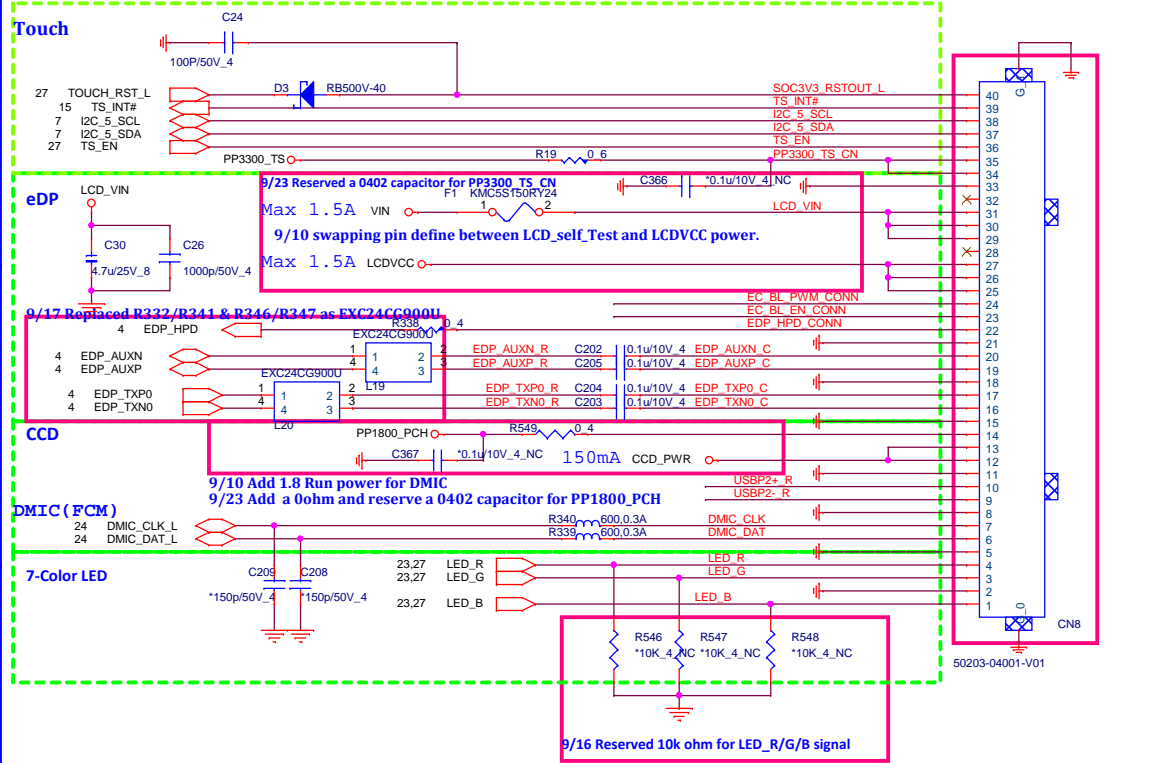
eDP panel control(LDS)



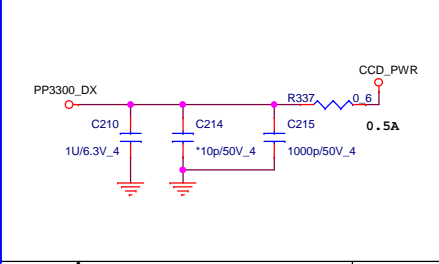
Touch Screen(TSN)



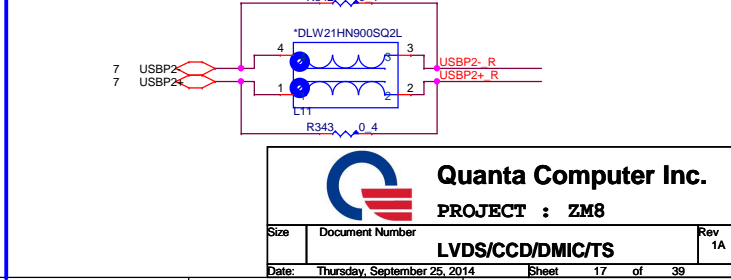
eDP(LDS)



CCD power(FCM)

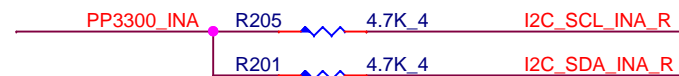
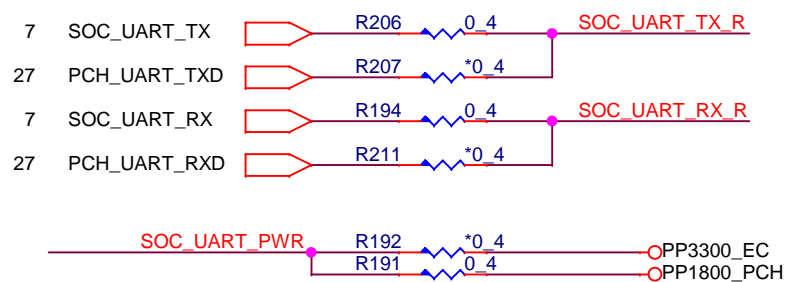


CCD USB(FCM)



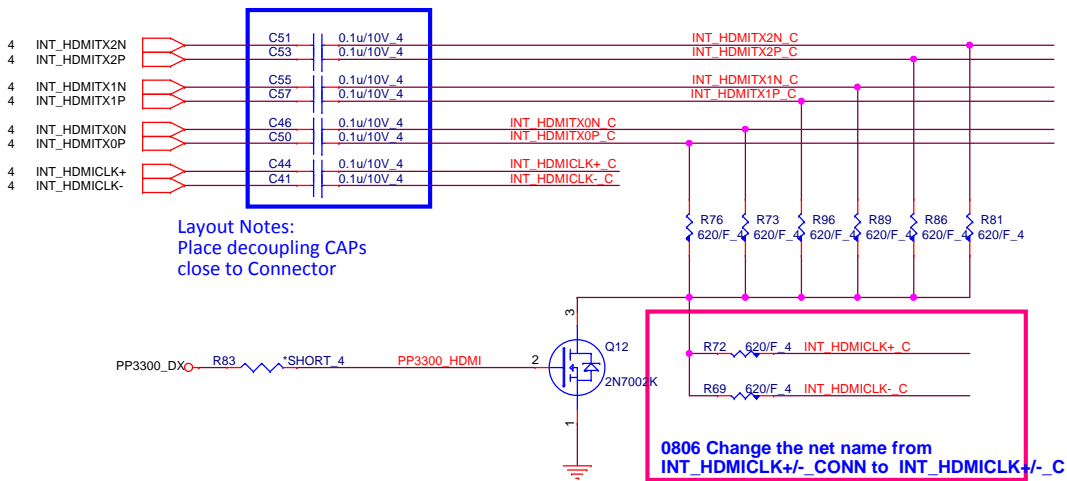
Socket part number AXK750147G

18

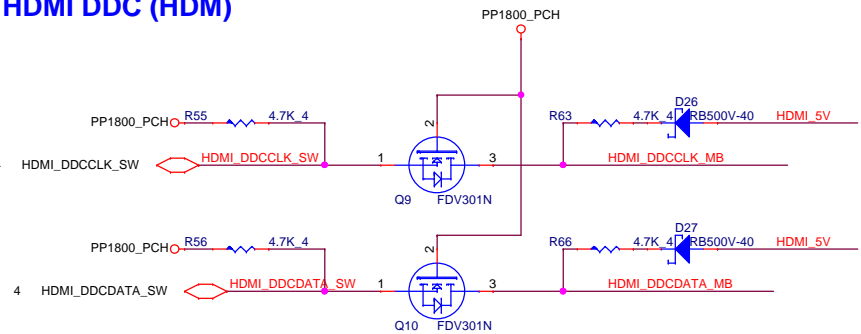


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	<b>Google Debug</b>	1A
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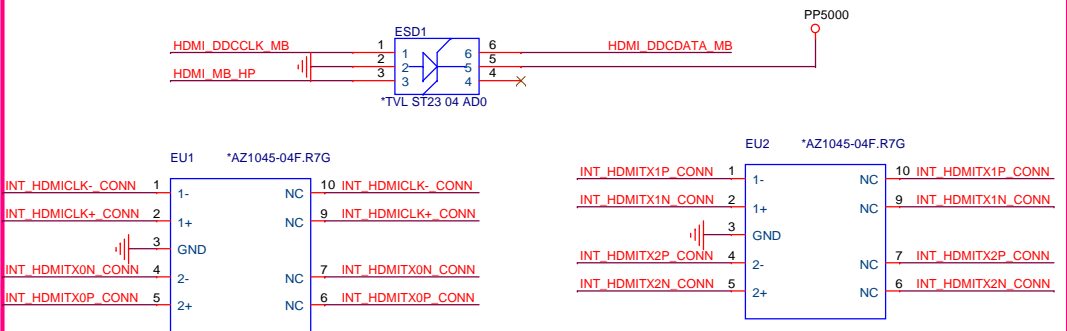
## HDMI Cost Reduced level shift (HDM)



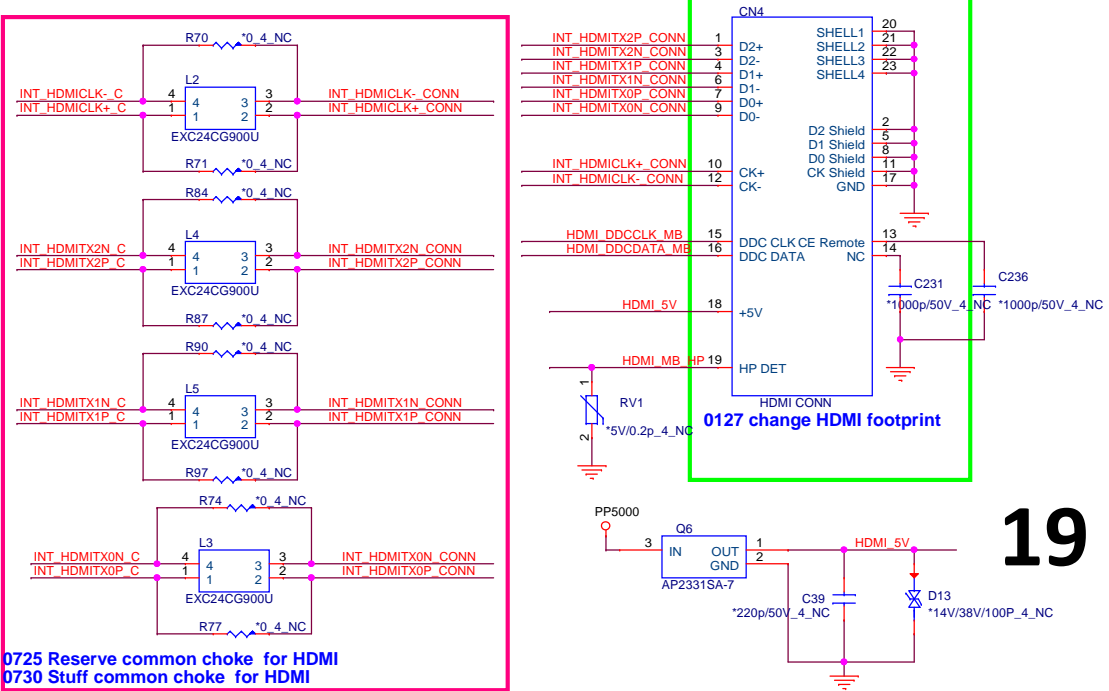
## HDMI DDC (HDM)



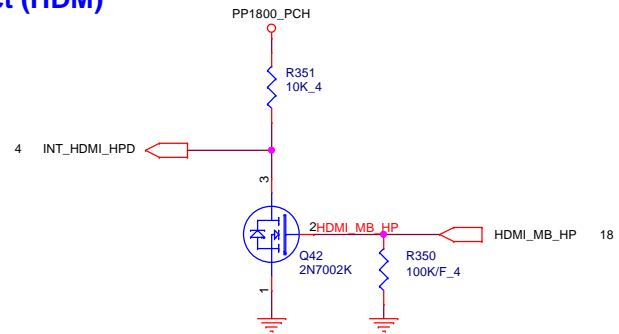
## For ESD



## HDMI connector (HDM)



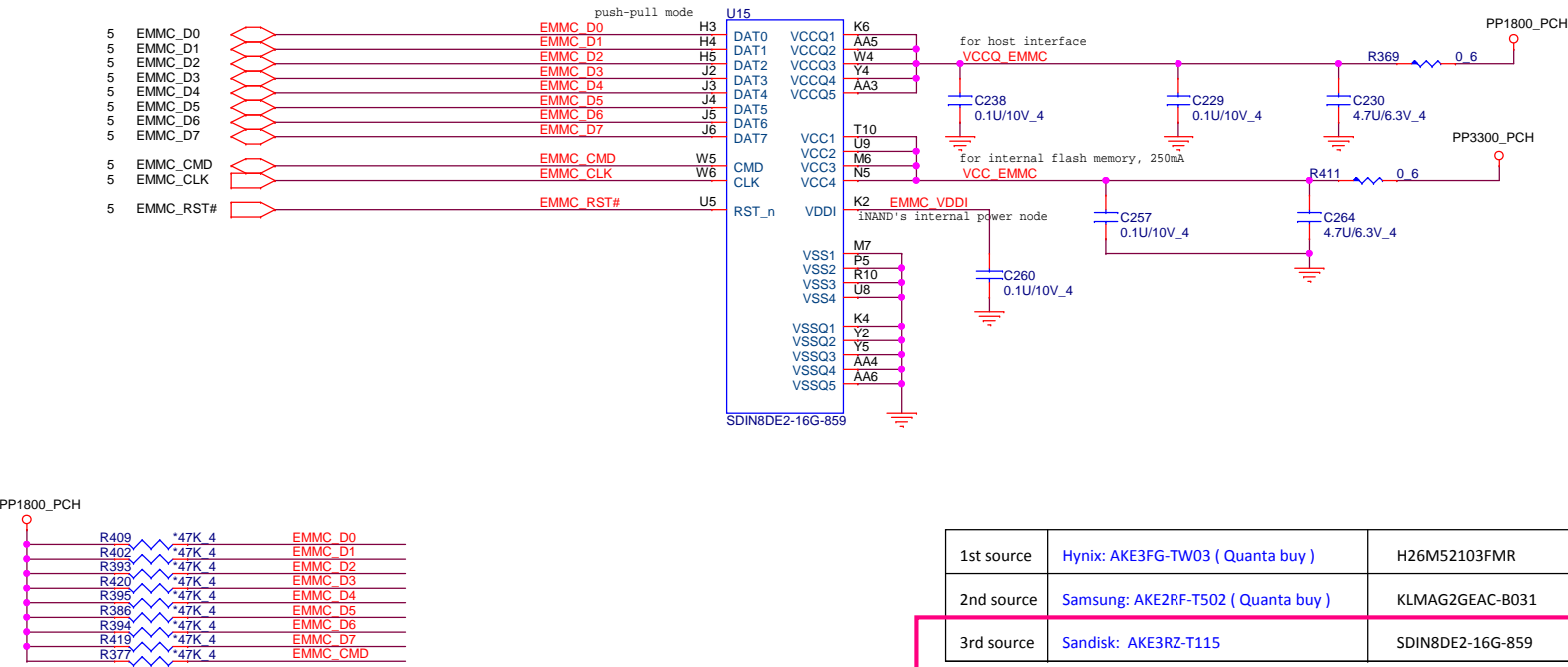
## HDMI-detect (HDM)





W/L 802.11A/B/G/N BT/FM MODULE AW-AM691N

EMMC (MMC)

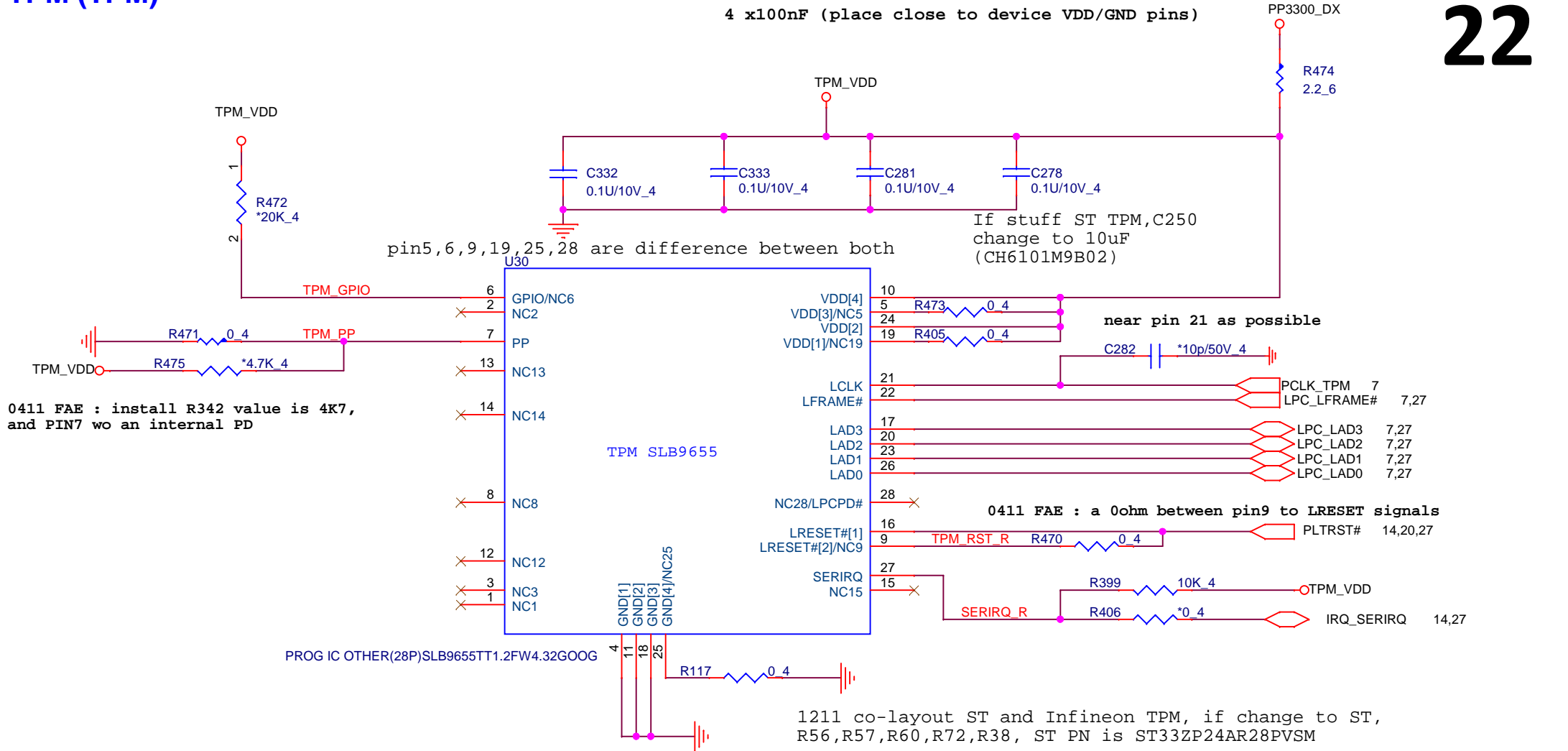


1st source	Hynix: AKE3FG-TW03 ( Quanta buy )	H26M52103FMR
2nd source	Samsung: AKE2RF-T502 ( Quanta buy )	KLMAG2GEAC-B031
3rd source	Sandisk: AKE3RZ-T115	SDIN8DE2-16G-859

9/25 Update new Sandisk EMMC QP/N: AKE3RZ-T115

# TPM (TPM)

22



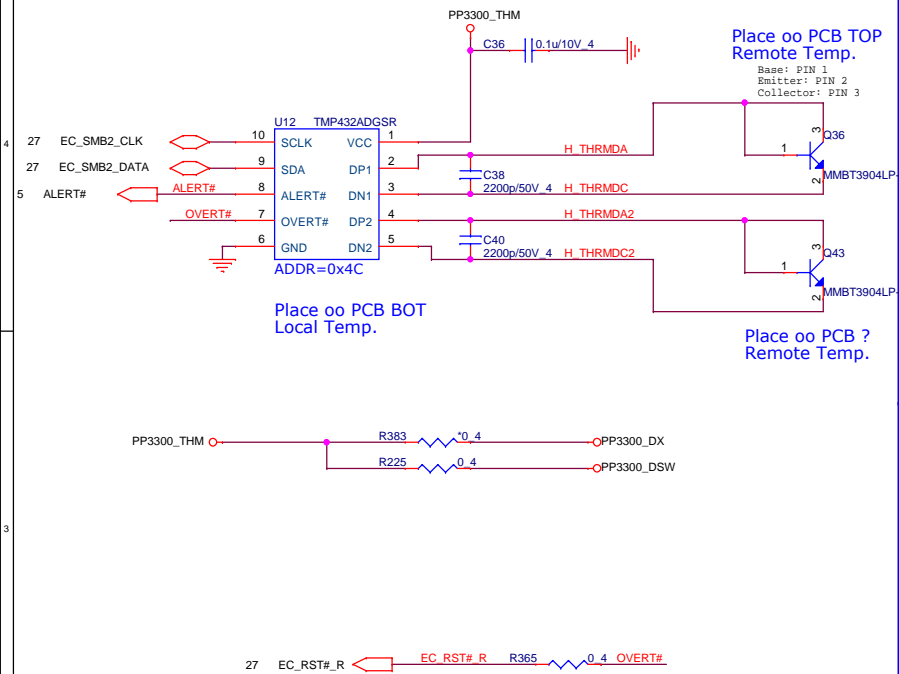
Quanta Computer Inc.

PROJECT : ZM8

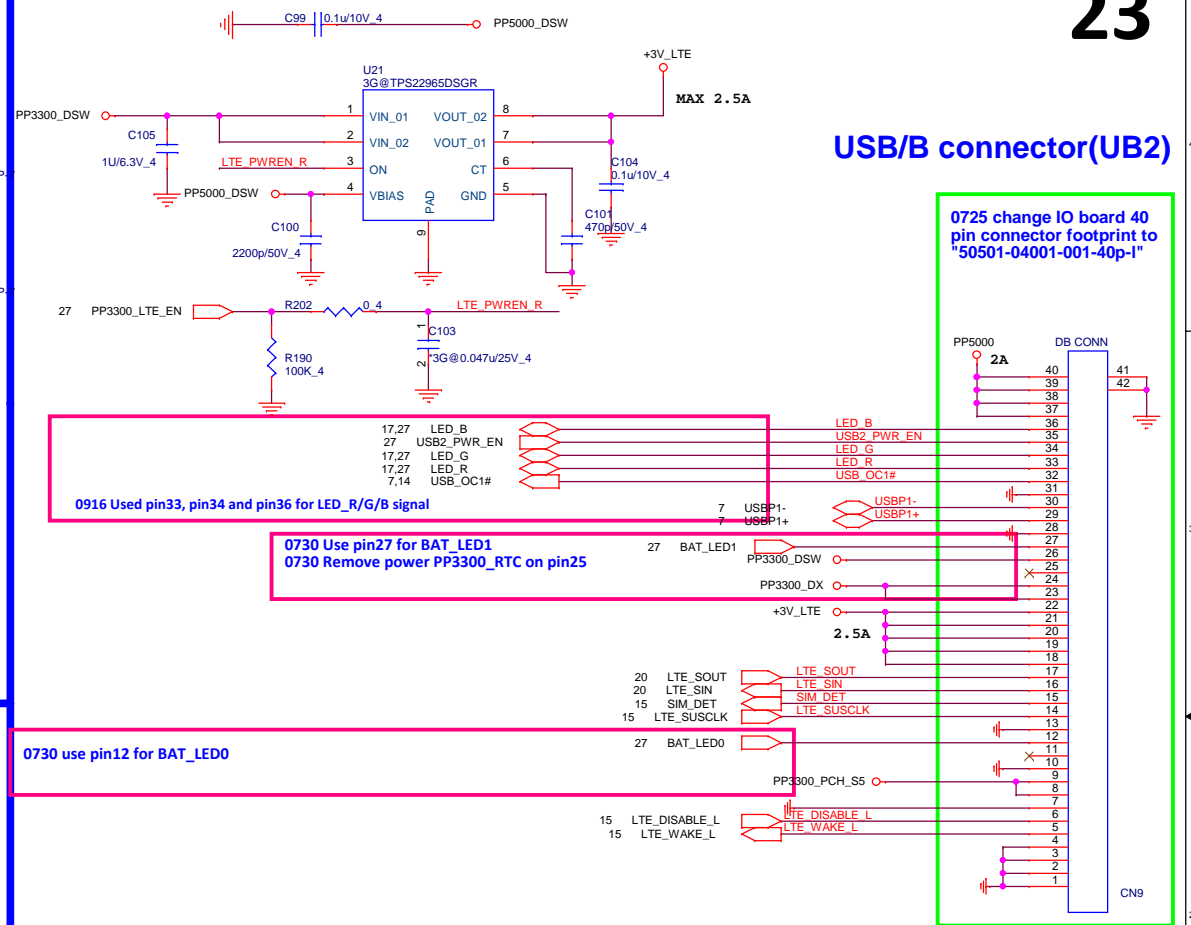
Size	Document Number	Rev
	TPM SLB9655	1A

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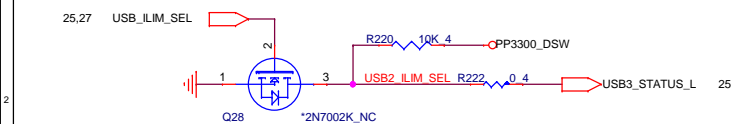
# Thermal Sensor(THM)



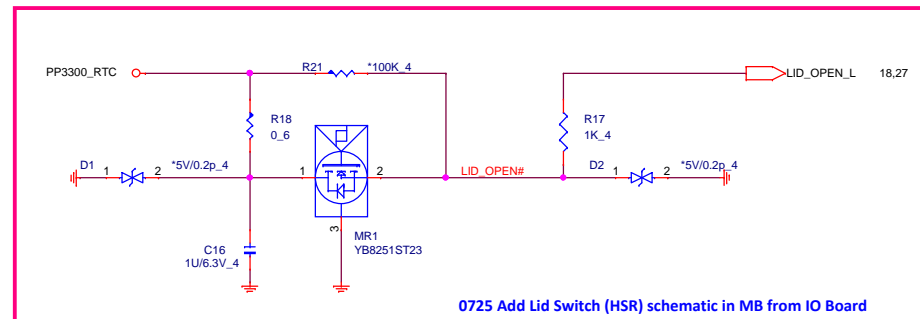
# LTE power switch(MNC)



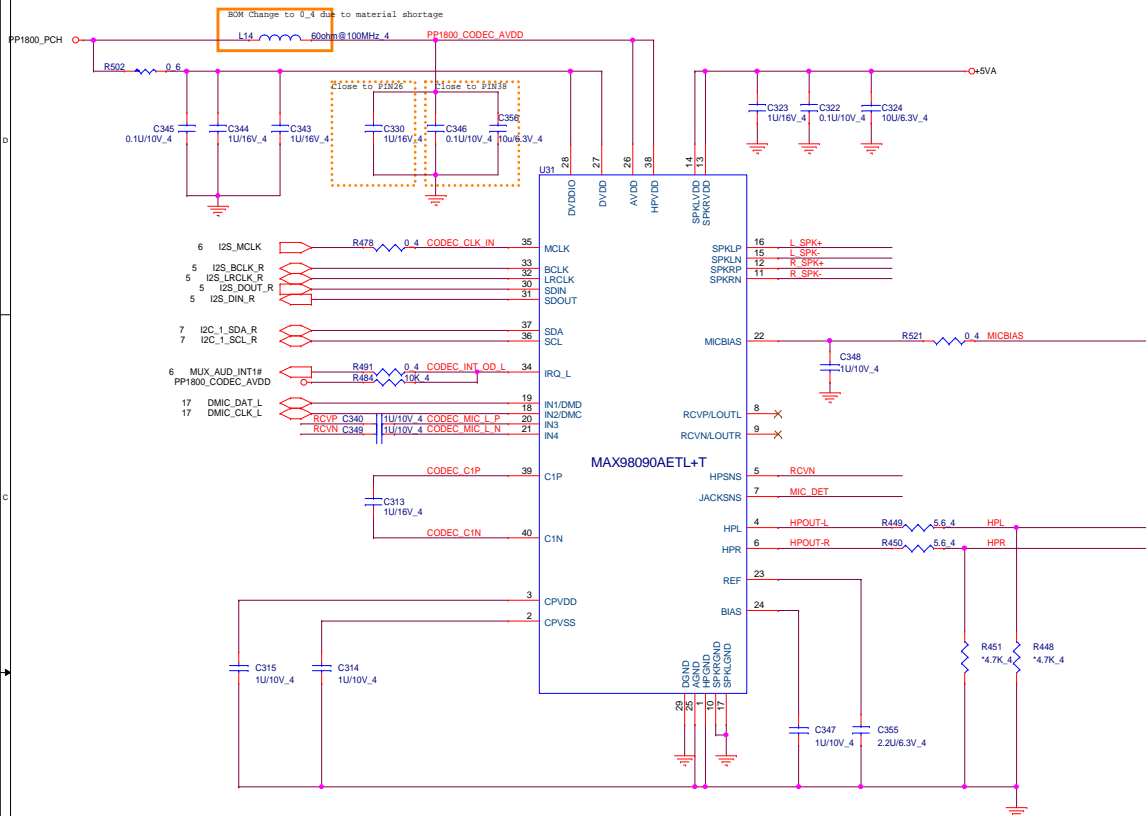
# USB Switch Current Control(UBC)



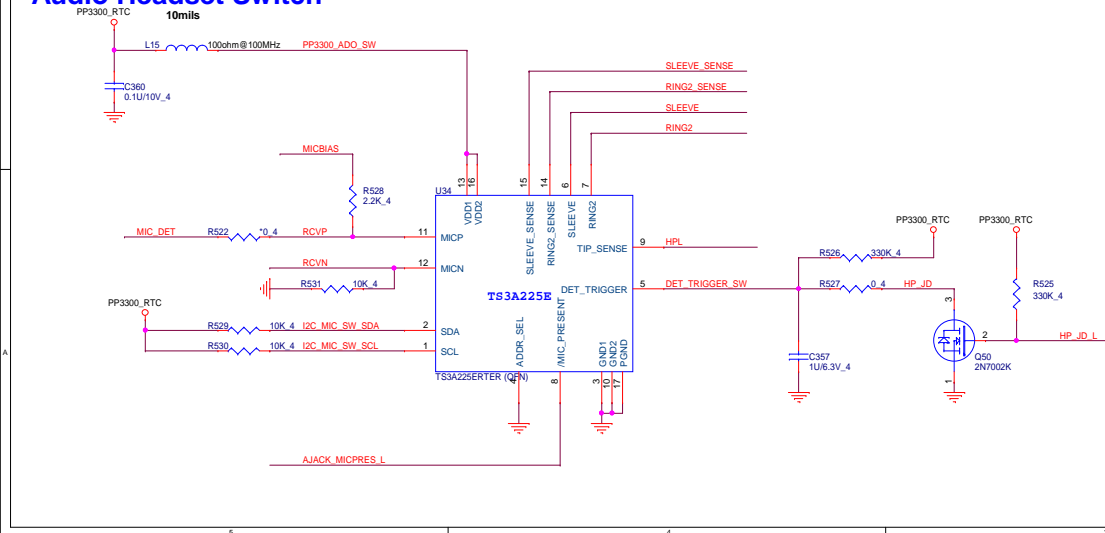
# Lid Switch (HSR)



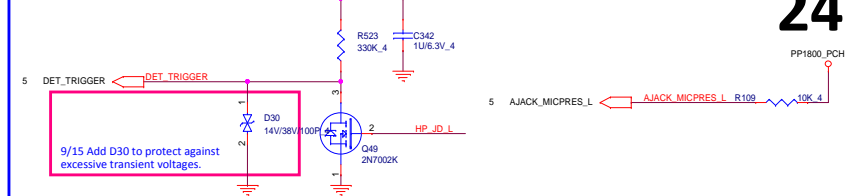
## AUDIO CODEC (ADO)



## Audio Headset Switch



## SOC DET(ADO)



## HEADPHONE/Mic combo(ADO)

combo jack  
Normal Open

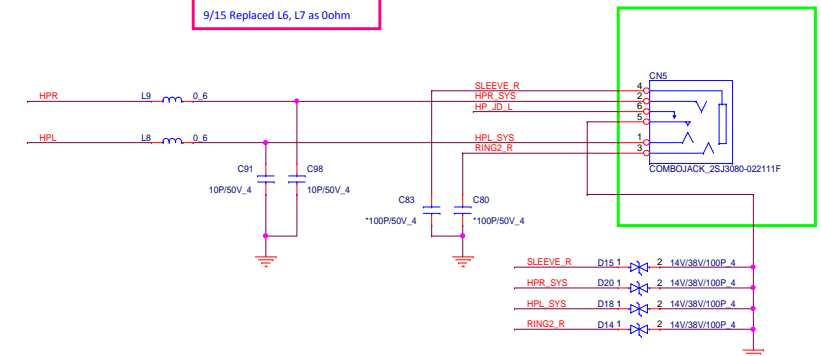
P/N: DFTJ06FR652  
Normal open

PIN1 --> L?

PIN2 --> R?  
PIN3 --> GND/MIC?

PIN4 --> MIC/GND?

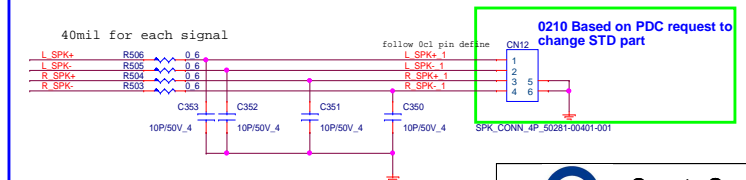
PIN5 --> JD?  
PIN6 --> GND?



## Codec PWR 5V(ADO)



## Internal Speaker(ADO)

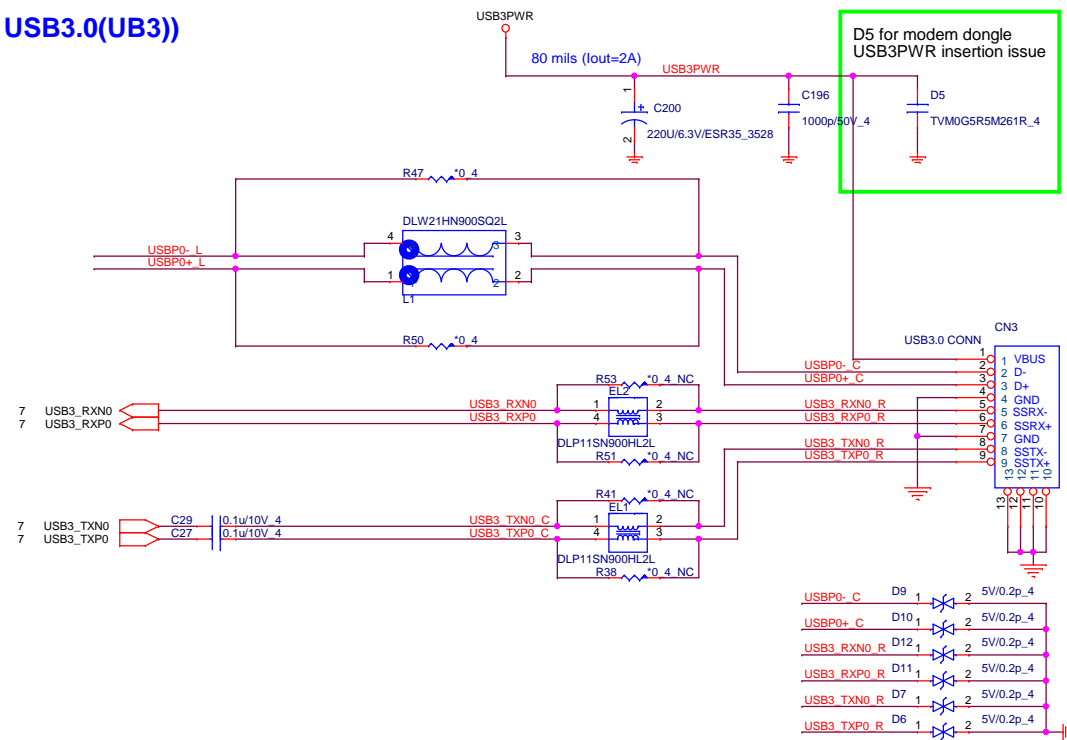


**Quanta Computer Inc.**

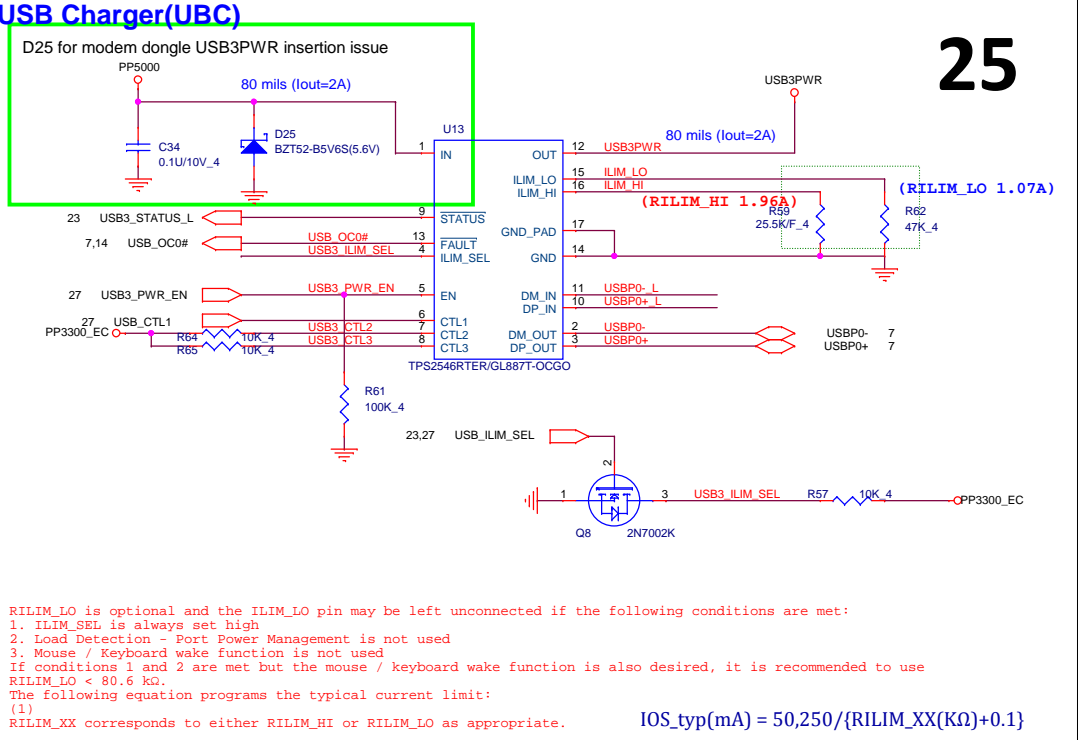
PROJECT : ZM8

Size	Document Number <b>MAX98090/HP/SPK</b>	Rev <b>1A</b>
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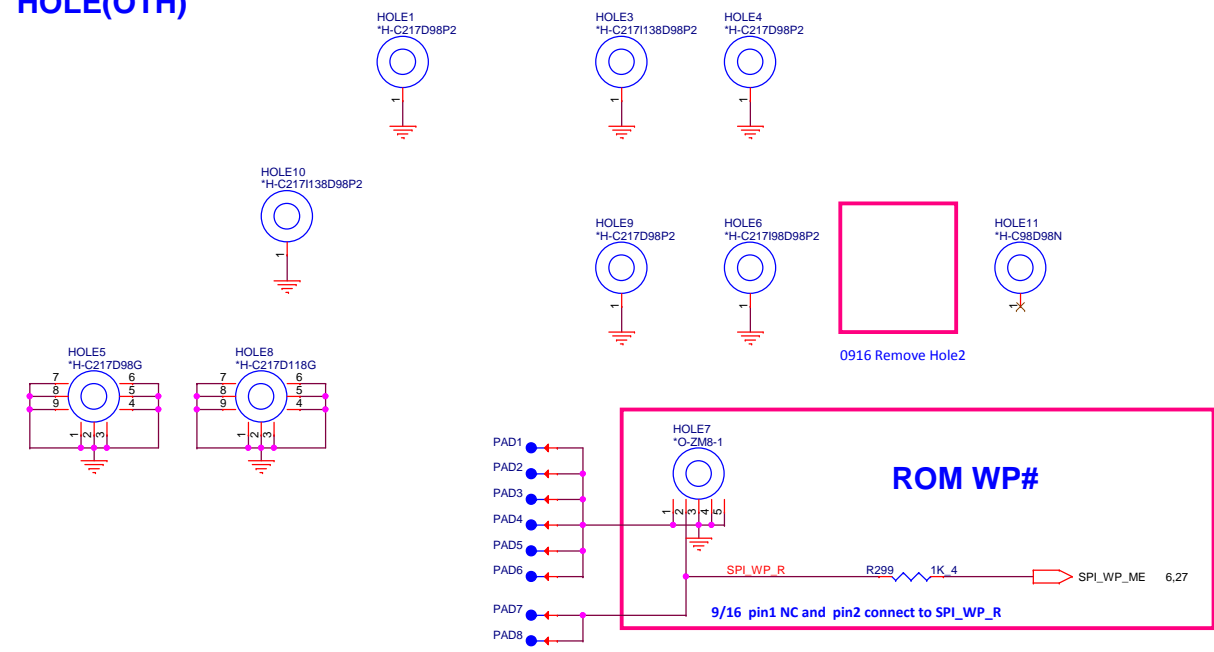
# USB3.0(UB3)



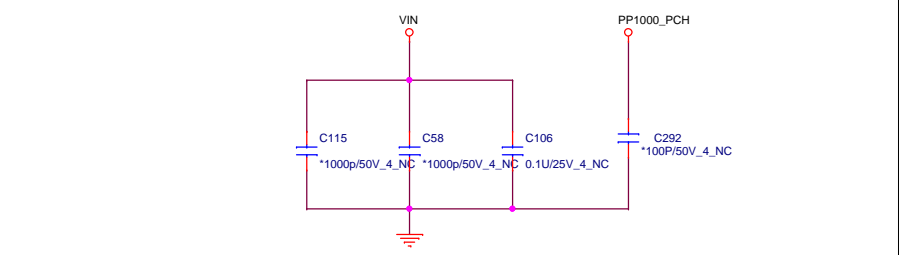
# USB Charger(UBC)



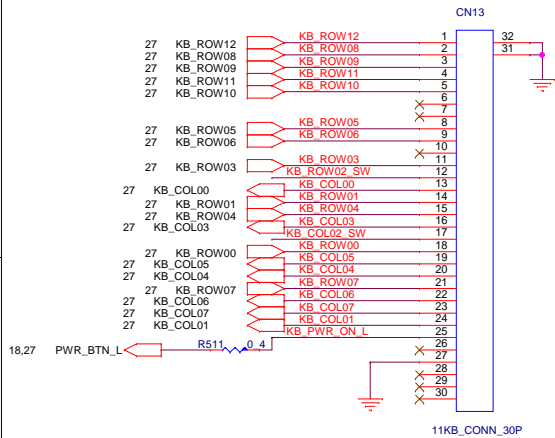
# HOLE(OTH)



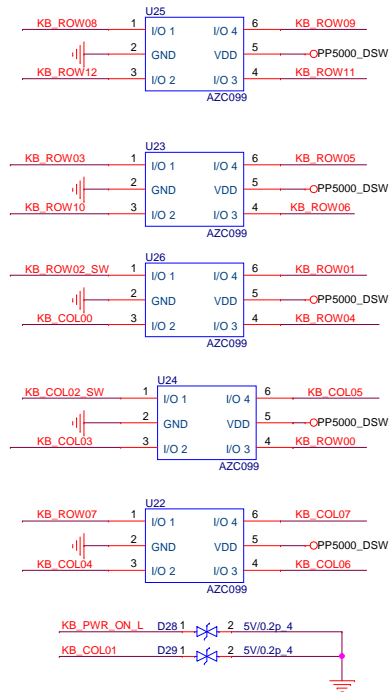
# EMI(EMC)



## K/B (KBC)

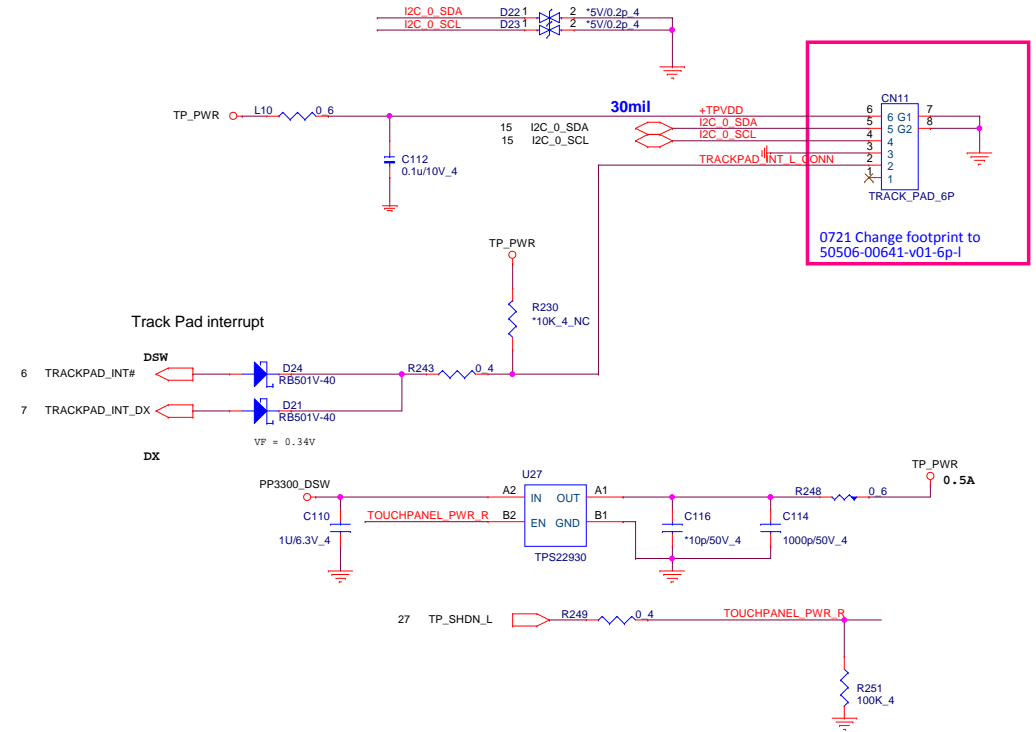


## K/B ESD (EMC)

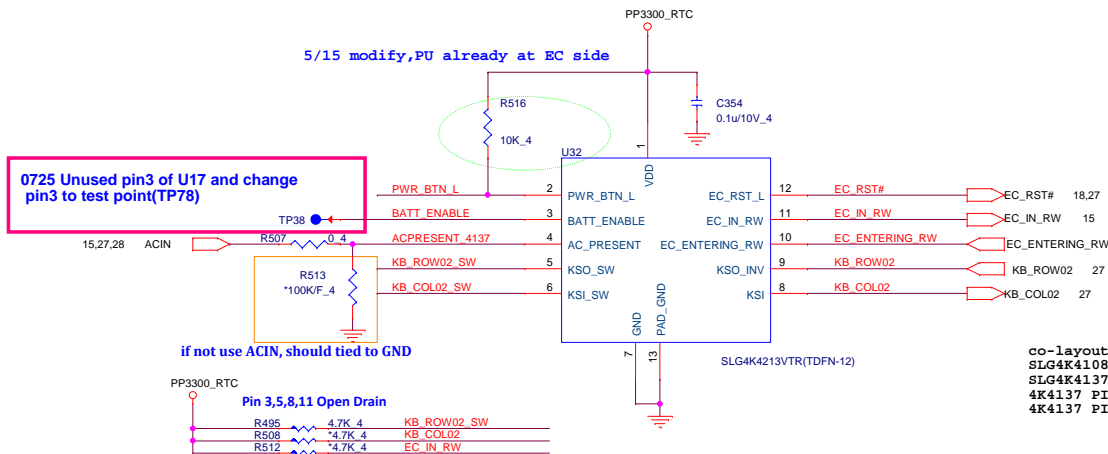


0220 Add and stuff ESD components on KB nets  
0221 swap pin of U1002-U1006 for layout

## Track PAD BOARD CONN (TPD)



0721 Change footprint to  
50506-00641-v01-6p-l

HOLELESS RESET  
2-CHIP(KBC)

Connect to EC reset pin  
Connect to GPIO on CPU  
with PU to GPIO power  
well  
Connect to EC pin C5 (must  
be low when EC IN RESET)

co-layout 4K4108 and 4K4137  
SLG4K4108 (AL004108000)  
SLG4K4137 (AL004137000)  
4K4137 PIN3 is BATT\_ENABLE  
4K4137 PIN4 is AC\_PRESENT

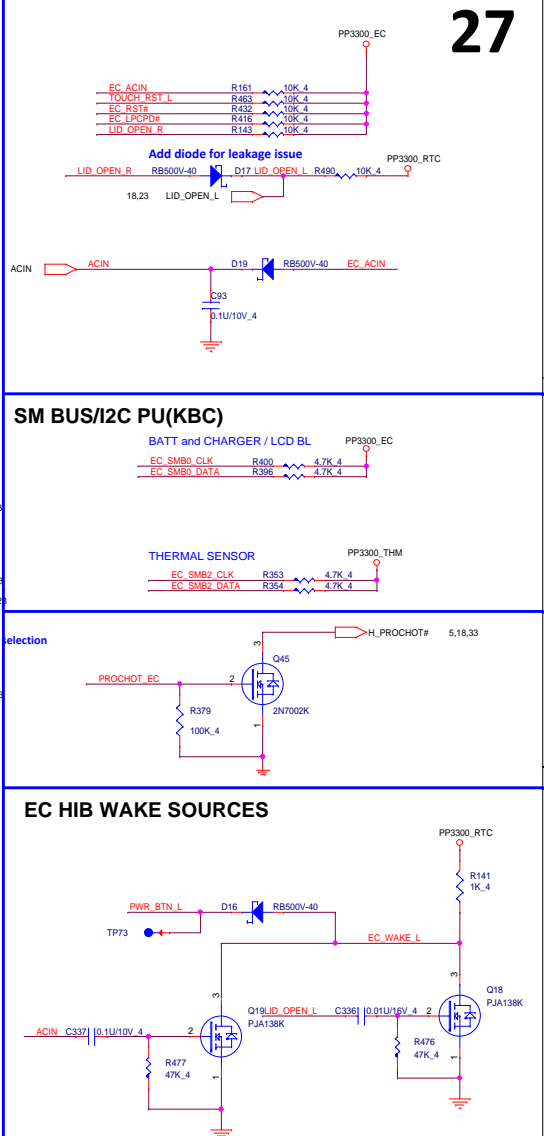


Quanta Computer Inc.


PROJECT : ZM8

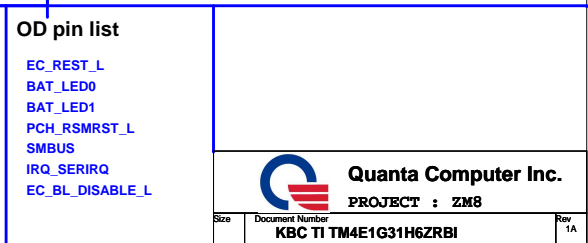
Size	Document Number	Rev
	KB/TP/FAN/HW Reset	1A

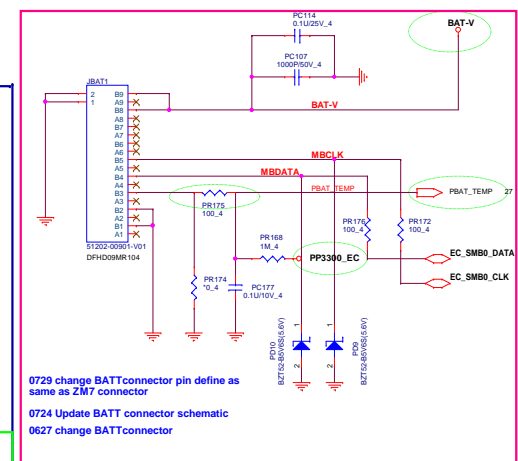
Date: Thursday, September 25, 2014 Sheet 26 of 39



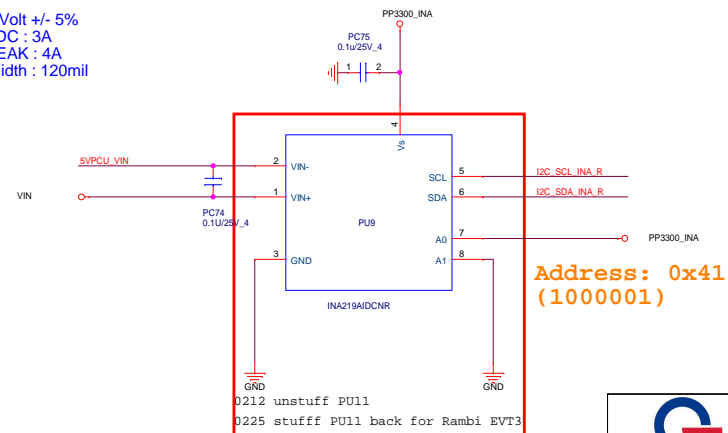
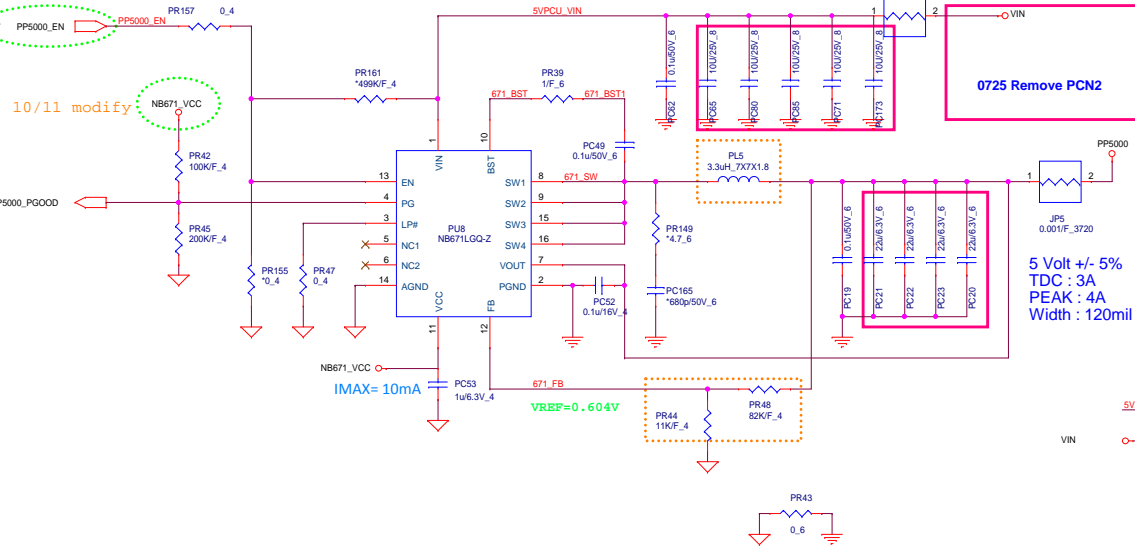
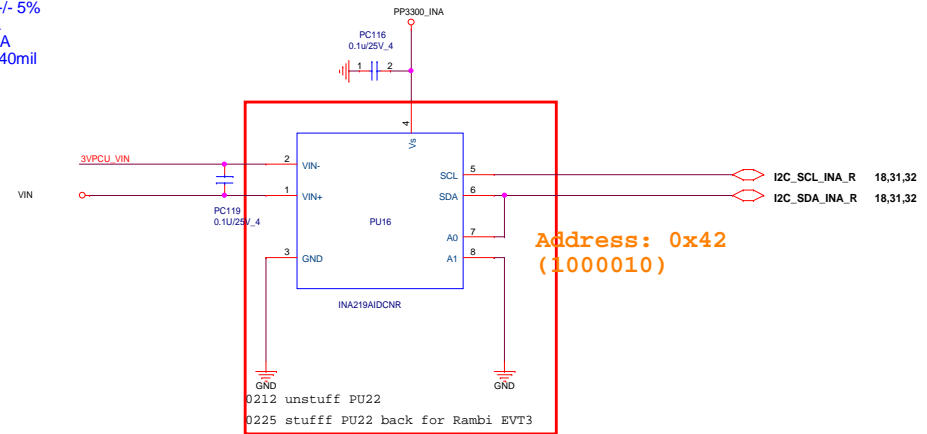
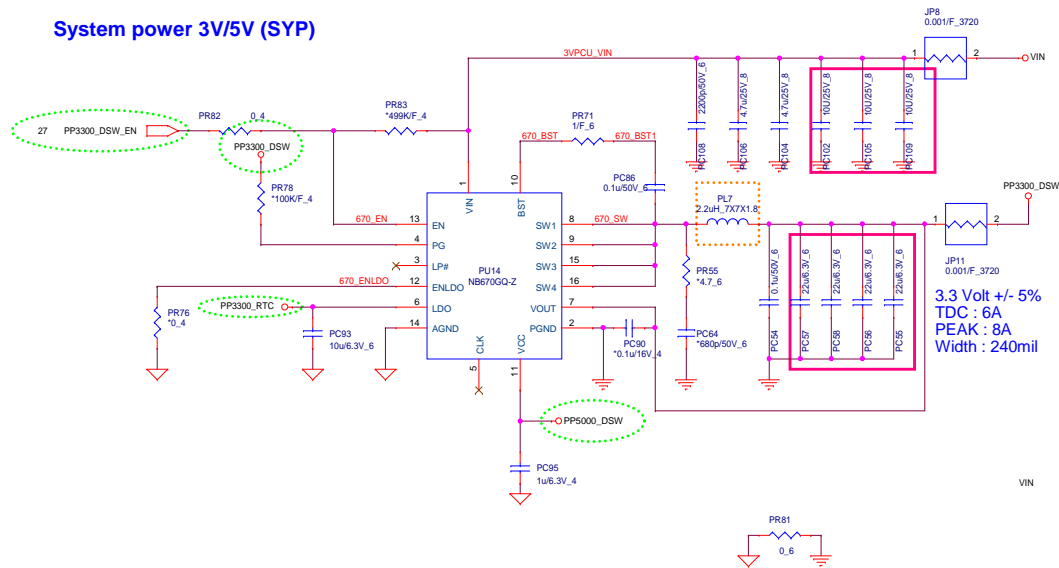
## HWPG(KBC)

15 PP3300\_PCH\_SS\_PG 





# System power 3V/5V (SYP)





**PROJECT :**

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# Memory core power (MCP)

TDC : 0.75A  
PEAK : 1A  
Width : 40mil

31

TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

PP1350\_VREF

+DDR\_VTT\_RUN

Greater than or equal 40mil

0916 Changed to CS+0107FA00 for layout placement

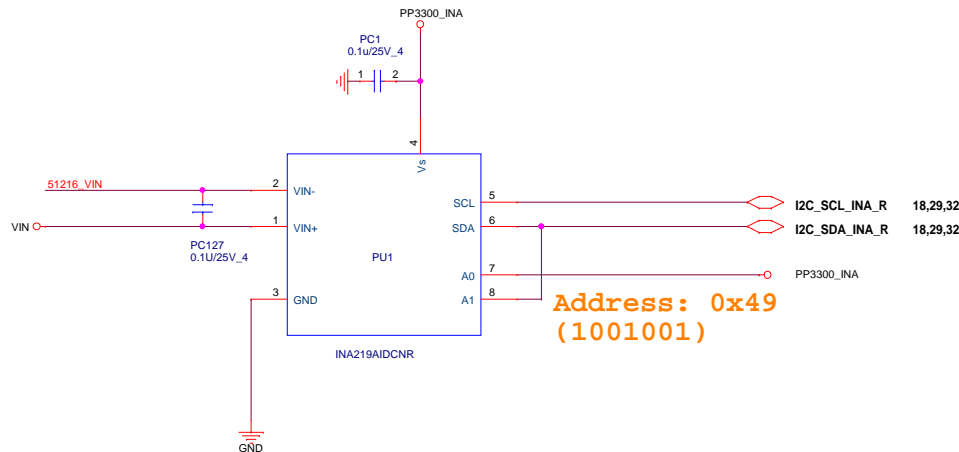
1.35 Volt +/- 5%  
TDC : 3.55A  
PEAK : 4.73A  
OCP : 6A  
Width : 160mil

Close to output cap

OCP=6A  
L ripple current  
= $(19-1.35) \times 1.35 / (2.2 \mu \times 400k \times 19)$   
=1.425A  
Vtrip=[ $6 - (1.425/2)$ ]\*14mohm  
=0.07402V  
Rlimit= $0.07402 / 10 \mu A \times 8 = 59.22k\Omega$

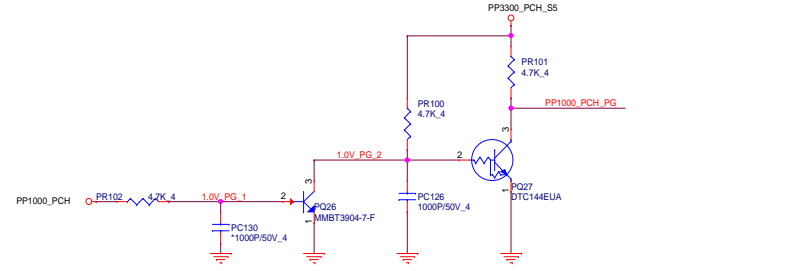
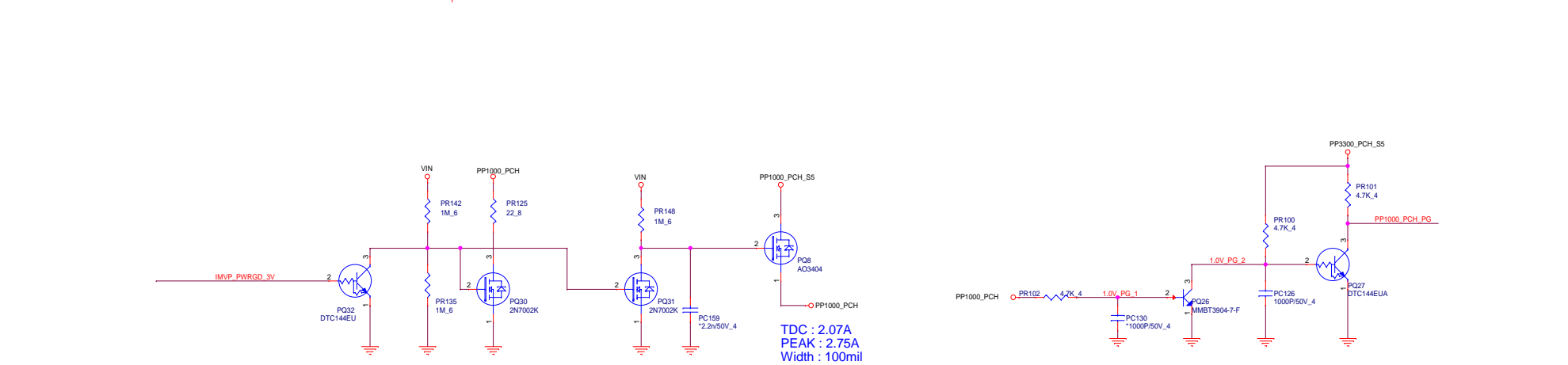
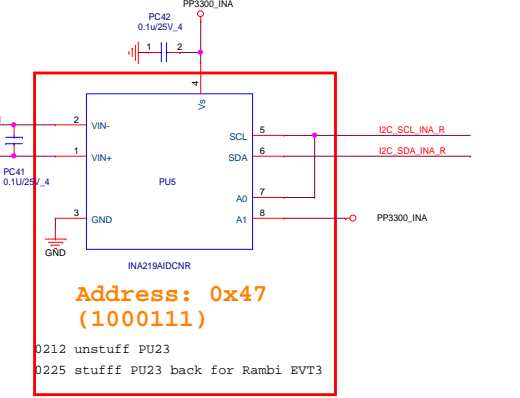
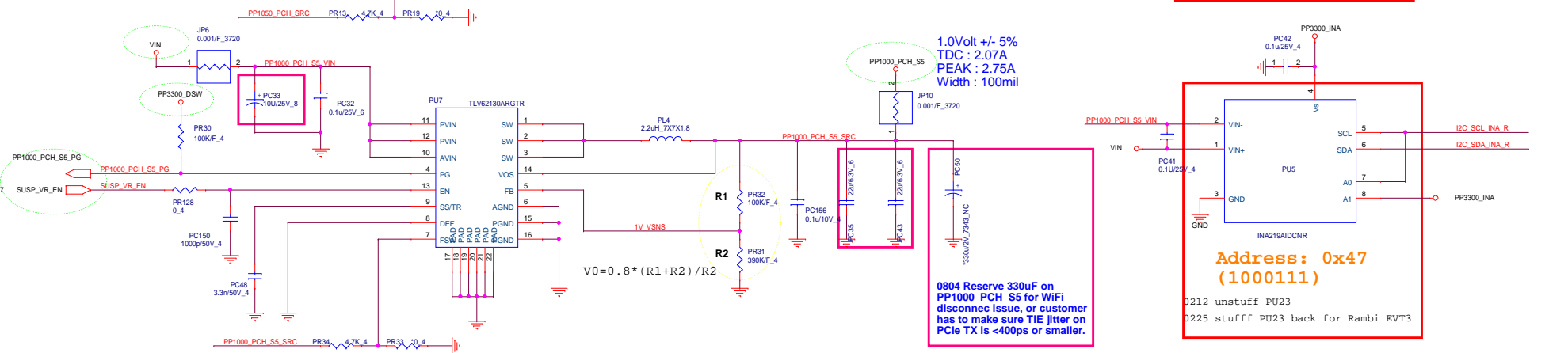
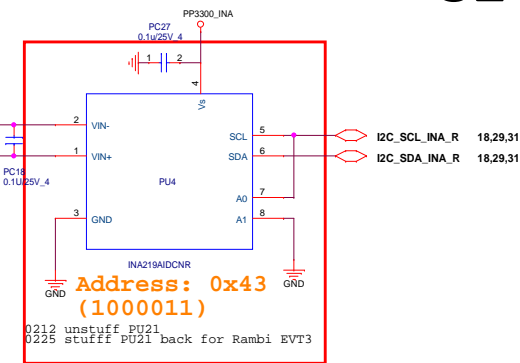
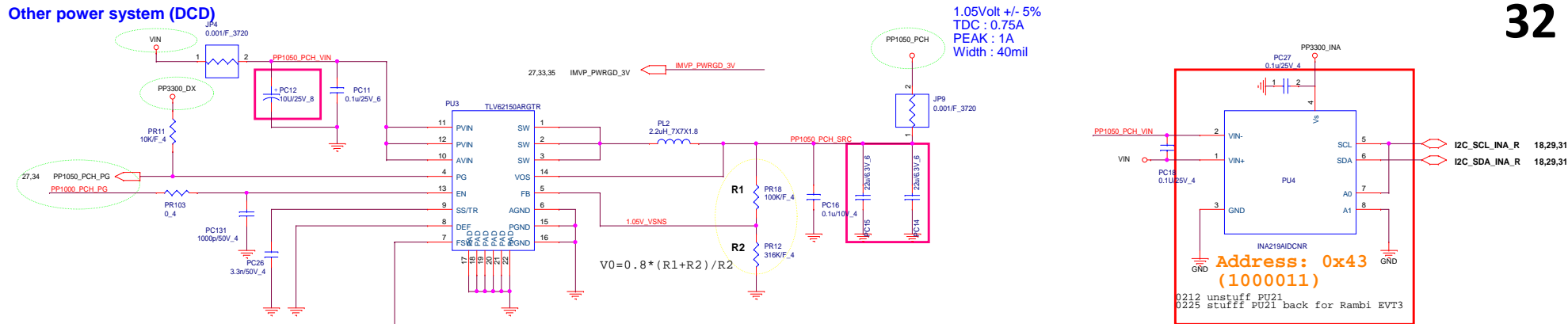
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

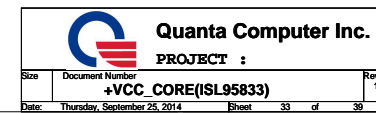
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



# Other power system (DCD)

32





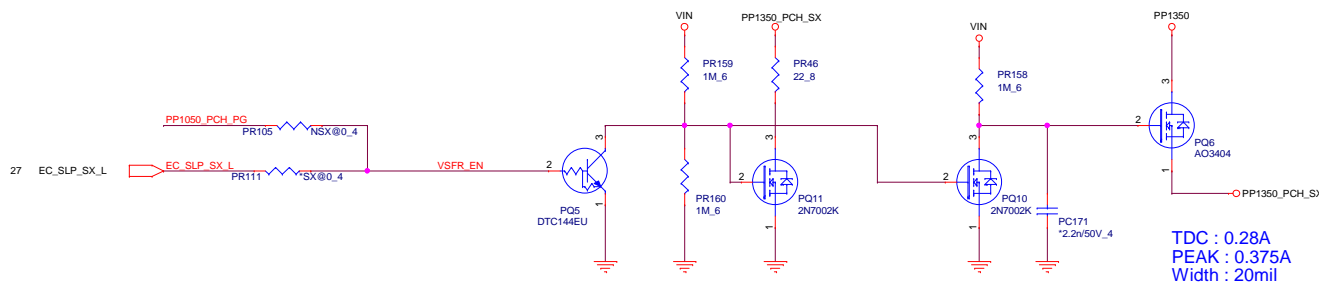
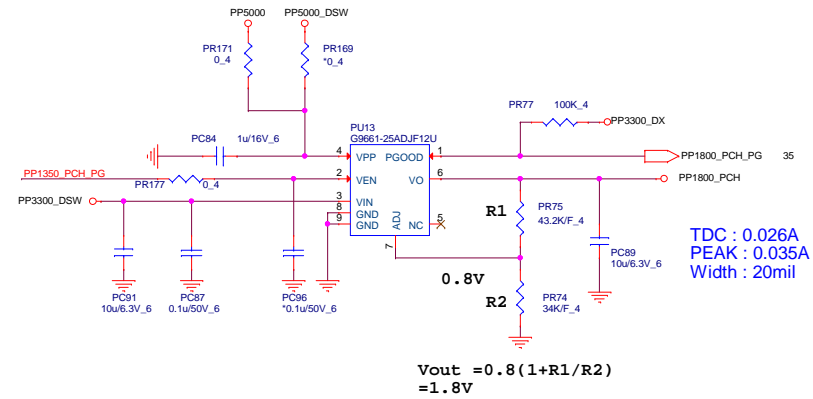
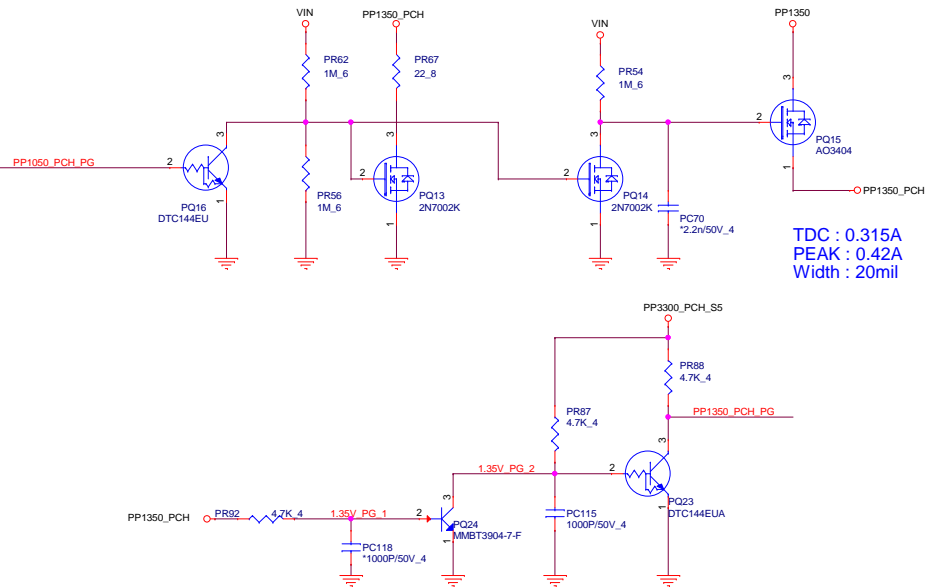
# Other power system (DCD)

34

31 VSFR\_EN

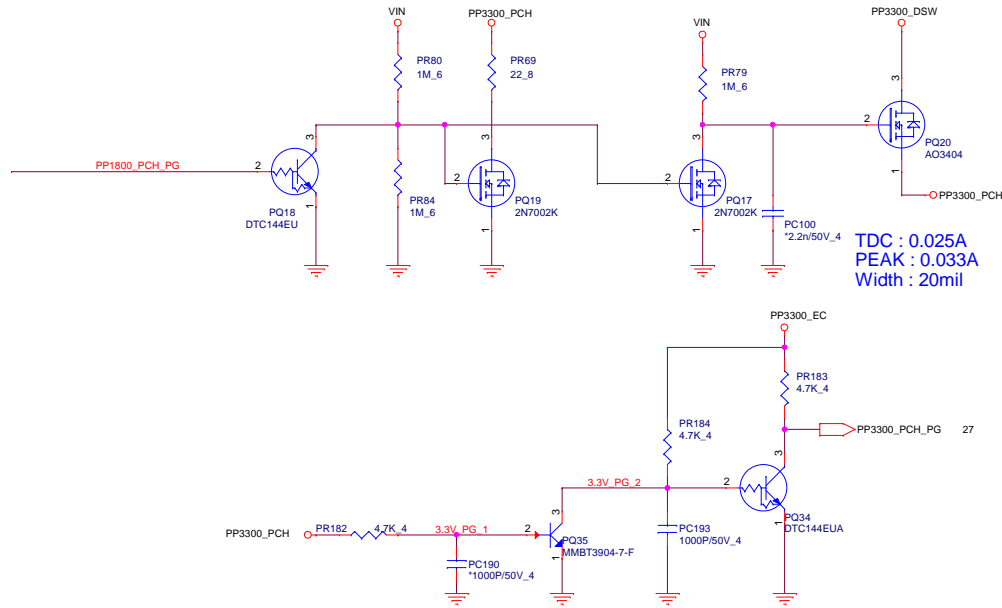
27,32 SUSP\_VR\_EN

27,32 PP1050\_PCH\_PG



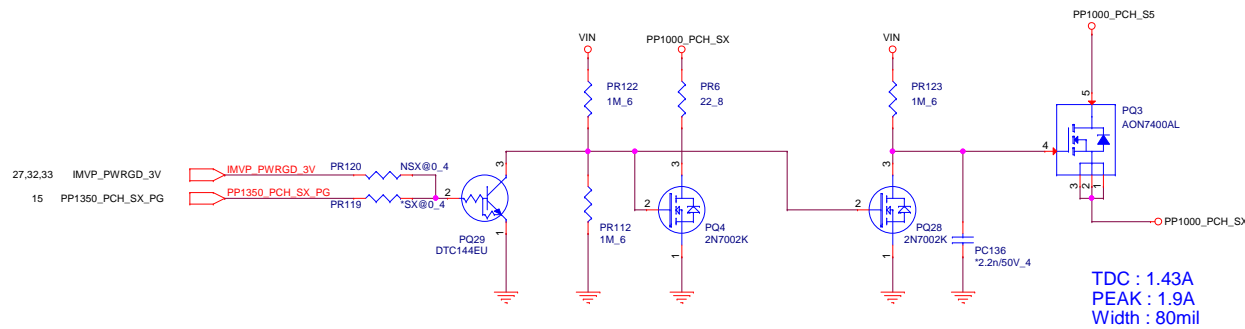
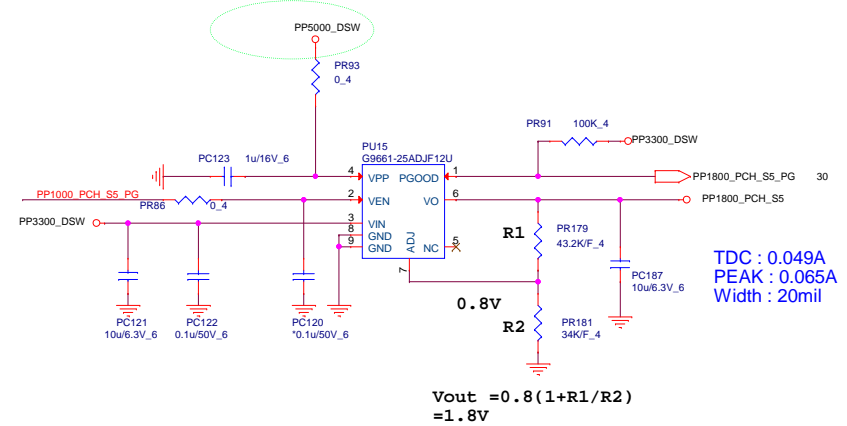
## Other power system (DCD)

35



0219 Change G9661 to TPS62243 for PP1800\_PCH\_S5

0220 change back to LDO for PP1800\_PCH\_S5

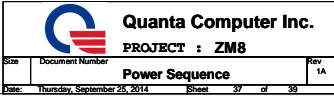




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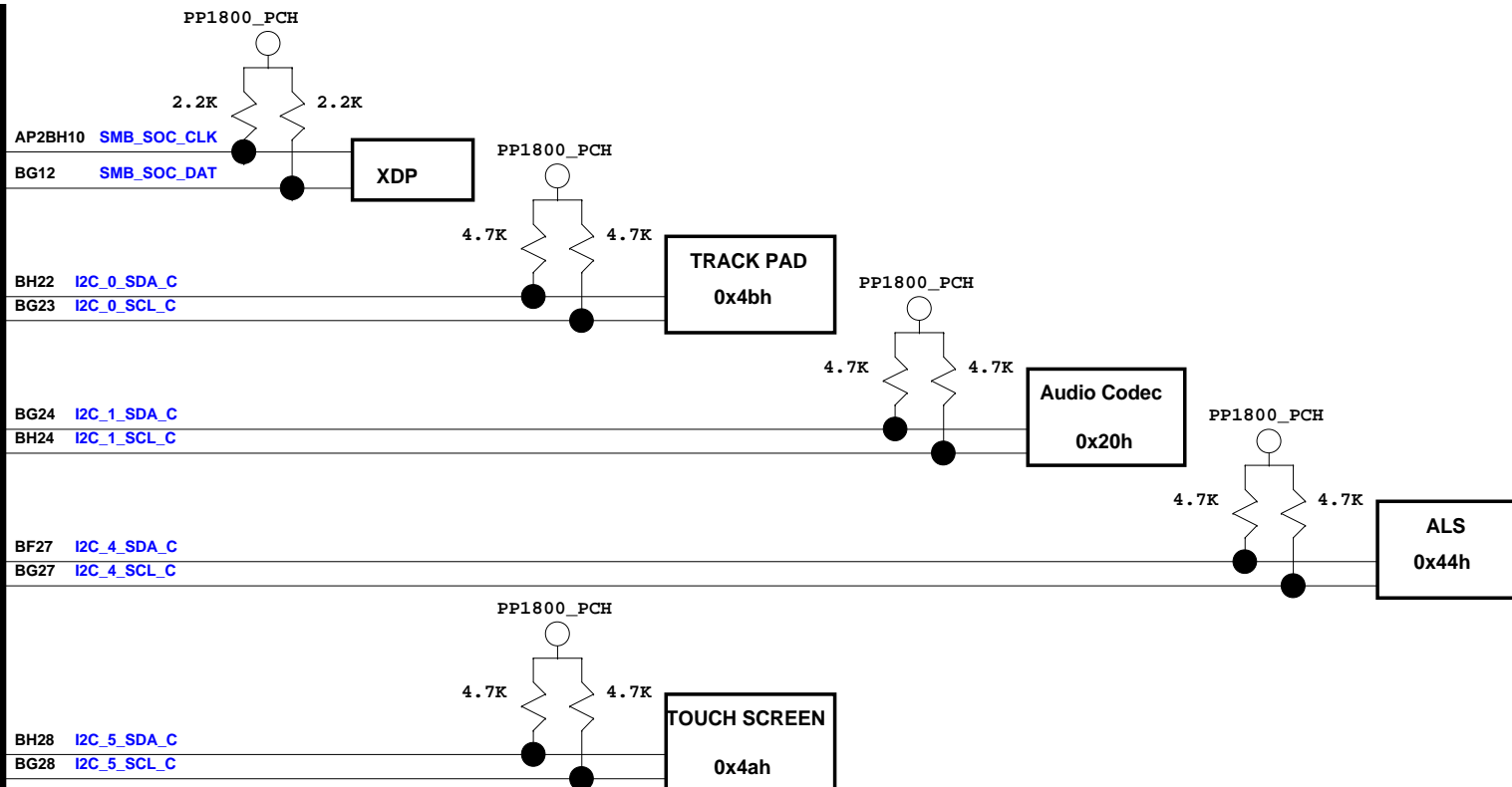
**PROJECT :**

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Thermal protect				
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**SMBUS**  
**Bay-trail M**

**I2C**



**KBC**  
**TI**  
**SMBUS**

